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High-Speed High-Voltage High-Current Power Transistors

This Manual is designed to provide a basic understanding of the theory and application of high-speed, high-voltage, and high-current power transistors. It covers physical theory, structures, geometries, packaging, safe-operating-area considerations, thermal fatigue, and the operation and requirements of power transistors in typical circuits that illustrate amplification, switching, and control applications. Selection charts are included to facilitate choice of the optimum type of power transistor for a variety of military, industrial, or commercial applications.

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Contents

General Physical Theory

Many of the electrical characteristics and ratings of a transistor are directly dependent upon the physical properties of the device. Among others, this group includes the transistor current-gain parameters alpha (α) and beta (β), emitter and collector efficiencies, base transport factor, voltage ratings, and transit and delay times.

CURRENT-GAIN PARAMETERS

Common-base current gain, α, is the ratio of collector current to emitter current (i.e., $\alpha = I_C/I_E$). Although α is slightly less than unity, circuit gain is realized as a result of the large differences of input (emitter-base) and output (collector-base) impedances. The input impedance is small because the emitter-base junction is forward-biased, and the output impedance is large because the collector-base junction is reverse-biased.

Common-emitter current gain, β, is the ratio of collector current to base current (i.e., $\beta = I_C/I_B$). Useful values of β are normally greater than ten.

The following relationship is apparent from Kirchoff's Law:

$$I_E = I_B + I_C$$

where I_E is the total current at the emitter junction, I_B is the current flowing into the emitter junction from the base, and I_C is the current flowing into the emitter junction from the collector.

From the definitions of α and β and Kirchoff's Law, the following relationship between α and β can be derived.

$$\beta = \frac{\alpha}{1-\alpha}$$

The common-base current gain α is determined by emitter efficiency γ base transport factor β_o, and collector efficiency α^* (generally, very near unity), as follows:

$$\alpha = \gamma\beta_o\alpha^*$$

EMITTER EFFICIENCY

In a forward-biased p-n-p transistor, holes from the emitter diffuse into the base, and electrons from the base diffuse into the emitter. The total emitter current, I_E is the sum of the hole-current component I_p and the electron current component I_n and, therefore, may be expressed as follows:

$$I_E = I_p + I_n$$

The potential collector current, I_C, is the difference between the drift currents and is given by

$$I_C = I_p - I_n$$

The electrons that diffuse from the base into the emitter originate in the base dc supply and add to the total base current. This electron current I_n, however, does not contribute to the collector current and, in effect, represents a loss in current gain that is directly attributable to poor emitter injection efficiency. The loss in current gain can be held to a minimum if the resistivity of the base is made

much greater than that of the emitter so that the number of free electrons in the base available to diffuse into the emitter is substantially smaller than the number of free holes in the emitter available to diffuse into the base.

BASE TRANSPORT FACTOR

If high emitter efficiency is assumed, the holes injected from the emitter into the base diffuse to the collector junction. However, some of these holes recombine with free electrons in the base and, in effect, are annihilated. Base current must flow to replenish the free electrons used in this recombination process so that the emitter-base forward bias is maintained. In other words, charge neutrality must prevail. For a high value of the base transport factor β_o, the lifetime of holes in the base (a function of the property of the material) must be long, or the time necessary for the holes to reach the collector must be short. Any reduction in the time required for the holes to reach the collector requires a decrease in base width or an increase in the accelerating field used to speed the holes through. The approximate relationships of the base transport factor, β_o, to base width and material properties for homogeneous-base and graded-base transistors are as follows:

1. For a homogeneous base,

$$\beta_o \approx 1 - \frac{1}{2}\left(\frac{W}{L}\right)^2$$

2. For a graded base (which has an aiding drift field),

$$\beta_o \approx 1 - \frac{1}{4}\left(\frac{W}{L}\right)^2$$

where W is the width of the base and L is the diffusion length of the injected carriers in the base. The value of L may be calculated from the following equation:

$$L = \sqrt{D\tau}$$

where D is the diffusion constant of the appropriate carrier in the base material and τ is the lifetime of the injected carriers in the base (time constant for annihilation of injected carriers).

The value of the base transport factor should be in the order of 0.98 for the transistor to provide useful gain.

VOLTAGE RATINGS

The collector-to-base or emitter-to-base breakdown (avalanche) voltage is a function of the resistivity or impurity doping concentration at the junction of the transistor. When there is a breakdown at the junction, a sudden rise in current (an "avalanche") occurs. In an abruptly changing junction, called a step junction, the avalanche voltage is inversely proportional to the impurity concentration. In a slowly changing junction, called a graded junction, the avalanche voltage is dependent upon the rate of change of the impurity concentration (grade constant) at the physical junction. Fig.1 shows the two types of junction breakdowns.

Collector Punch-Through Voltage

The collector voltage can be limited below its avalanche breakdown value if the depletion layer (space-charge region) associated with the applied collector voltage expands through the thin base width and contacts the emitter junction. The

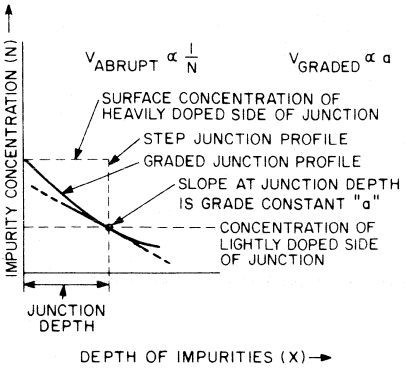


Fig. 1 — Step-junction and graded-junction breakdown.

doping in the base (under the emitter) and the base width in relation to the magnitude of applied voltage govern whether punch-through occurs before avalanche. Higher doping concentrations and wider bases increase punch-through voltage V_{PT} in accordance with the following relationship:

$$V_{PT} = \frac{qNW^2}{2kE_o}$$

where q is the electronic charge, N is the doping-level concentration in the base, W is the base width, k is the dielectric constant, and E_o is the permittivity of free space (kE_o is approximately 1 X 10^{-12} farad per centimeter for silicon).

Collector-to-Emitter Voltages

The collector-to-emitter voltages are governed by the magnitude of the collector-to-base voltage and the current-gain multiplication factors. Fig. 2 shows a family of collector-emitter voltages for different emitter-base resistances (R_{BE}).

The relationship of collector-to-emitter voltage V_{CEO} to collector-to-base voltage V_{CBO} and current gain a follows from the effects of carrier ionizations in crossing the collector depletion region. More collector current flows than

is collected at the base-collector junction by an amount determined from the rate at which charge carriers are being

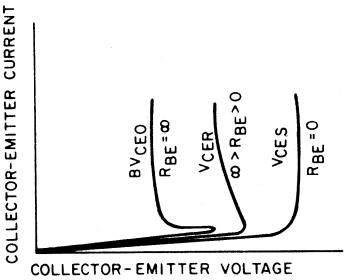


Fig. 2 – Collector-to-emitter voltage as a function of collector-to-emitter current for different emitter-to-base resistances.

ionized and accelerated across the depletion region. If the additional amount of current is arbitrarily represented by the expression CI_C, and the current gain is expressed as $I_C = \alpha I_E$, then $CI_C = C\alpha I_E$. For high fields in which ionization is significant, the total current gain is represented by

$$I_C = \alpha I_E + C\alpha I_E = (1 + C)\, \alpha I_E$$

where the factor (1 + C) is normally referred to as the multiplication number M. The equation for the collector current, therefore, may be rewritten as follows:

$$I_C = M \alpha I_E$$

The collector-to-emitter reverse current I_{CEO} is related to the collector-to-base reverse current I_{CBO} and the current gain β as shown by the following equation:

$$I_{CEO} = (\beta + 1)\, I_{CBO}$$

(The relationship for the current I_{CEO} is derived from the expression $I_E = \beta I_B + I_B$, in which $I_B = I_{CBO}$ for the V_{CEO} condition).

It is apparent from the above relationship that, when β approaches infinity (at $M = 1/\alpha$), I_{CEO} also approches infinity, which is a condition for V_{CEO}.

For a given collector-to-emitter voltage, the multiplication factor M may be determined as follows:

$$M = \frac{1}{1 - (V/V_B)^n}$$

where V is the collector-to-emitter voltage, V_B is the collector-to-base voltage at breakdown (i.e., the collector-to-base avalanche voltage), and n is the avalanche factor.

Under the conditions for which collector-to-emitter voltage breakdown with the base open occurs, the following substitutions may be made in the equation for the factor M:

$$V = V_{CEO}$$
$$V_B = V_{CBO}$$
$$M = 1/\alpha$$

When these substitutions are made, the resultant equation can be solved for the collector-to-emitter breakdown voltage V_{CEO} to obtain the following result:

$$V_{CEO} = \frac{V_{CBO}}{(\beta + 1)^{1/n}}$$

For silicon p-n-p transistors, the avalanche factor n is approximately equal to 4; for silicon n-p-n transistors, this factor is approximately equal to 2.

CUT-OFF FREQUENCY

For all transistors, there is a frequency f at which the output signal cannot properly follow the input signal because of the time delays in the transport of the charge carriers. There are three principal cut-off frequencies, shown in Fig. 3, that may be defined as follows:

$f_{\alpha b}$ the base cut-off frequency, is that frequency at which alpha, α, is down 3 dB from the low-frequency alpha.

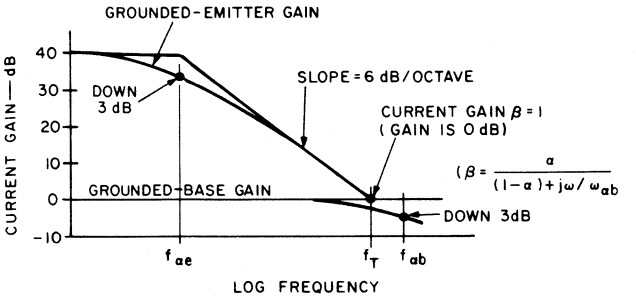


Fig. 3 – Cut-off frequencies.

$f_{\alpha e}$, the emitter cut-off frequency, is that frequency where beta, β, is down 3 dB from the low-frequency beta.

f_T is the frequency at which beta theroretically decreases to unity (zero gain) with a theoretical 6-dB per-octave drop. This term, which is useful figure of merit for transistors, is referred to as the gain-bandwidth product.

The frequency f_T at which beta (β) theoretically decreases to unity is related to transistor time delays by the following expression:

$$f_T \cong \frac{1}{2\tau \Sigma t_d}$$

where Σt_d is the sum of the emitter-delay time constant t_e, the base transit time t_b, the collector depletion-layer transit time t_{xm}, and the collector-delay time constant t_c.

Emitter-Delay Time

The emitter delay time is the time required to charge the capacitance, C_{Te}, of the emitter-base transition region through the emitter resistance r_e. The smaller the product of C_{Te} and r_e, the smaller the delay time. For a small value of C_{Te}, a small emitter area and a high base resistance are needed. The emitter-delay time constant, therefore, is expressed as follows:

$$t_e = r_e C_{Te}$$

Base Transit Time

The base transit time t_b is the time required for the injected carriers to diffuse and drift across the base width W. It is related to the average speed of the carriers and the width of the base. For a homogeneous base, this transit time is determined by the following equation:

$$t_b = \frac{W^2}{D}$$

The diffusion constant D, in turn, is related to the average carrier velocity (mobility) as follows:

$$D = \frac{\mu KT}{q}$$

where μ is the carrier mobility and kT/q is a temperature-dependent constant.

For short base transit time, narrow base width and a high carrier mobility are required.

Collector Depletion-Layer Transit Time

The collector depletion-layer transit time, t_{xm}, is the time required for the carriers to be swept through the collector depletion layer by the collector field. The collector delay time is related to the width of the depletion layer (xm) and the speed of the carriers (v). The speed, in turn, is governed by the applied field (E), up to a limiting or saturation velocity (v_{sc}). The relationship of transit time to the saturation velocity is given by the following equation:

$$t_{xm} = \frac{xm}{v_{sc}}$$

For silicon, v_{sc} is approximately equal to 8.5×10^6 centimeters per second at a value of E greater than 10,000 volts per centimeter.

Collector-Delay Time Constant

The collector-delay time constant t_c is the time required to charge the capacitance of the collector junction (C_{Tc}) through the combined series resistance from the emitter to the collector. Generally, only the collector series resistance (r_{sc}) is significant. The collector-delay time constant, therefore, is approximated by the following equation:

$$t_c = r_{sc}\, C_{Tc}$$

A reduction in the value of the collector resistivity causes an over-all decrease in the collector-delay time constant because r_{sc} is decreased more than C_{Tc} is increased. Also, small collector areas may help reduce t_c if r_{sc} is not grossly affected. The relationship of the collector area A to the series resistance r_{sc}, the collector resistivity ρ_c, the thickness of the collector ℓ, and the collector-junction capacitance C_{Tc} is shown in the following equations:

$$r_{sc} = \frac{\rho_c \ell}{A}$$

and

$$C_{Tc} = A\sqrt{\rho_c}$$

Physical Theory of Power Transistors

The physical theory of power transistors is complicated by the large current densities and high collector fields involved. In addition to any thermal effects and to the gain relationships discussed in the preceding section, physical properties of power transistors must be broadened to include three additional effects, as follows:

(a) base-conductivity modulation,
(b) current crowding,
(c) base widening.

BASE-CONDUCTIVITY MODULATION

Base-conductivity modulation is an effect that results in reduced gain of the transistor because of an increase in the base conductivity induced from the high density of the injected carriers from the emitter. As the conductivity ratios of the emitter and base shift, more base majority carriers are injected into the emitter. The increased density of the injected carriers greatly affects the ratio of hole current collected (for a p-n-p transistor) to the total emitter current. The relationship is shown by the following equation:

$$\gamma \approx \frac{I_p}{I_n + I_p}$$

where, as indicated previously, γ is the emitter injection efficiency, I_p is the hole current, and I_n is the electron current.

For low-current operation, I_p is related to I_n by the ratio of the emitter majority-carrier impurity concentration to the base majority-carrier impurity concentration. For a typical, well-designed transistor, I_n is negligible compared to I_p.

For high-current operation, I_n increases to levels that approach those of I_p (because of recombination and the requirement for charge neutrality in the base region). This effect reduces γ and substantially decreases gain. (If $I_n = I_p$, then $\gamma = 0.5$ and $\beta = 1$.)

The necessity for charge neutrality in the base requires that the base majority carriers (n_{base}) increase with an increase in the injected emitter carriers in accordance with the following equation:

$$n_{base} = \frac{J_E}{qV_{base}} + n_{Bo}$$

where J_E is the emitter current density, n_{Bo} is the initial base majority concentration of impurity, V_{base} is the diffusion- and drift-dependent base voltage, and q is the electron charge constant. This equation defines the change of base current I_n from the increase in base majority carriers (n_{base}) with current density J_E and relates its impact on γ.

The rate of recombination is also affected by the presence of increased carriers at higher injection levels which decrease the base transport factor β_o.

If it is assumed that there are no base-recombination effects, the shape of the curve in Fig. 4 is governed by the effects of current density on the injection efficiency in accordance with the following equation:

$$\beta = \frac{\sigma_{eo}}{\sigma_{Bo}\left(1 + \frac{J_E}{qVn_{Bo}}\right)}$$

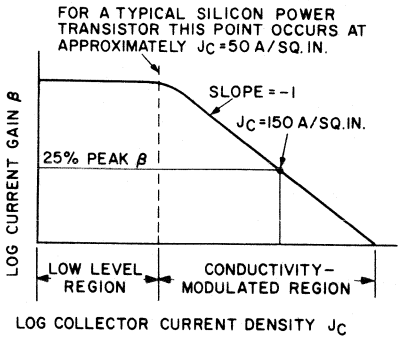


Fig. 4 — Current gain as a function of collector-current density. (In this diagram, the effects of recombination in the base are neglected.)

where β is the common-emitter current gain, σ_{eo} is the initial conductivity of the emitter, σ_{Bo} is the initial conductivity of the base, J_E is the emitter current density, q is the electronic charge constant, V is the carrier velocity of the base, and n_{Bo} is the concentration of initial base impurity doping.

For low-current operation, β is equal to β_1. If qVn_{Bo} is treated as the base modulation constant, K_2, the value of β at a moderate emitter current density J_E is given by

$$\beta = \frac{K_2 \beta_1}{J_E}$$

A graphic representation of this equation (log β as a function of log J_E) shows that β varies with a slope of -1. For a minimum of conductivity-modulation effects, the initial base concentration n_{Bo} should be as high as practicable with good low-level gain. Also, current density should be low; therefore, the emitter area should be large.

CURRENT CROWDING

The effect of current crowding causes a reduction in the usable gain of a power transistor because of the electrical

sistors with heavily doped collectors, provided that the current density is the same for both types of transistors. The mechanism for reduced gain results from effects on the base transport factor caused by the widened or extended base width and charge pile-up in the vicinity of the collector-base junction.

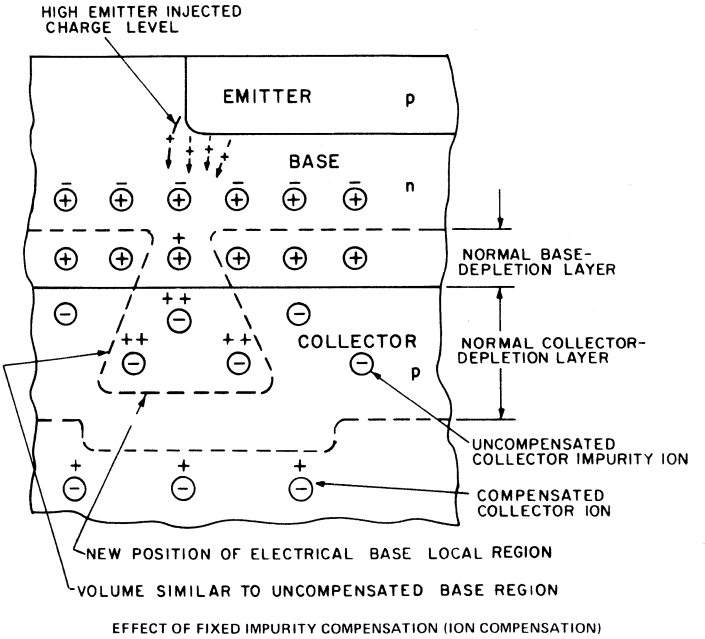


Fig. 7 – Effect of fixed-impurity compensation (ion compensation,

Structures, Geometries, and Packaging

In power transistors, structure refers to the junction depth, the concentration and profile of the impurities (doping), and the spacings of the various layers of the device. Geometry refers to the topography of the transistor. These factors and the method of packaging have an important bearing on the types of applications in which a power transistor can be used to optimum advantage. The proper choices and trade-offs among these factors are required to obtain high-speed, high-voltage, or high-current capabilities for power transistors.

STRUCTURES

Various structures have been developed to provide different electrical, thermal, or cost properties, with each having certain advantages or compromises to offer. Table I lists the principal structures available for silicon power transistors, together with some of the advantages and disadvantages of each type.

Alloy Transistors

In alloy transistors, impurities are applied directly to the top and bottom surfaces of a carefully prepared slice, or wafer, of silicon. The wafer is then subjected to controlled

Table I - Types of Structures for Silicon Power Transistors

Structure	Advantages	Disadvantages
Alloy	Generally rugged	Low speed, high cost
Hometaxial-base	Rugged, low cost	Low speed
Double-diffused mesa	High speed	Poor saturation resistance
Double-diffused planar	High speed, low leakage	Poor saturation resistance
Triple-diffused mesa	High speed, low-saturation resistance	Moderate cost, moderate leakage
Triple-diffused planar	High speed, low leakage, low saturation resistance	Moderate to high cost
Double-diffused epitaxial mesa	High speed, low-saturation resistance	Moderate cost, moderate leakage, less rugged
Double-diffused epitaxial planar	High speed, low leakage, low saturation resistance	Higher cost, less rugged
Epitaxial-base mesa	Moderate speed, low saturation resistance	Low voltage, moderate leakage
Multiple epitaxial-base mesa	Moderate speed, low saturation resistance, rugged, high voltage	Moderate cost
Double-diffused multiple-epitaxial mesa	High speed, rugged, low saturation resistance	Moderate cost, moderate leakage

conditions until the impurity forms an actual metallurgical alloy with the silicon wafer, as shown in Fig. 8.

The alloy fronts form an abrupt (step) junction with the base on both sides. For this type of junction, the base

resistivity must be high to support the collector voltage rating. This high resistivity accounts for the extremely wide base width needed to limit punch-through effects. Lifetime must be high in the base to provide adequate gain with the wide base. Relatively low junction-forming temperatures permit preservation of the high initial lifetime of the silicon wafer.

The collector is mounted (soldered) directly to a heat sink to provide the necessary thermal performance. Simple solder contacts are used to make connections with the base (surrounding the emitter) and the emitter directly on top of the deposited impurity.

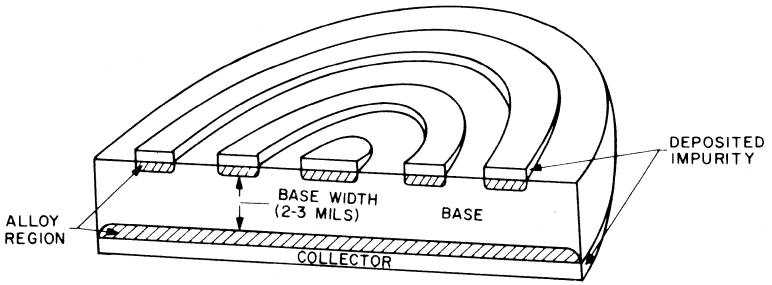


Fig. 8 – Alloy-transistor structure.

The principal advantage of the alloy transistor is its extremely rugged junctions which can withstand repeated high-energy power pulses. This electronic ruggedness results because the very wide base width employed causes the charge carriers to fan out (diffuse) as the carriers travel from the emitter to the collector. In addition, because of the wide base, the transit time of the carriers through the base is relatively long, and lower frequency response and longer switching time results.

Hometaxial-Base Transistors

Hometaxial-base transistors start with a wafer of moderately-high-resistivity silicon on which are deposited several thin layers of impurities. Then, under controlled

conditions, the impurities are driven deep into both sides of the silicon wafer. Early in the diffusion, the process is interrupted briefly, and a mesa or raised portion is selectively etched to define an emitter geometry. The process is complete when the deep diffused junctions are separated by a moderately wide (about 1 mil) base region. Fig. 9 shows the

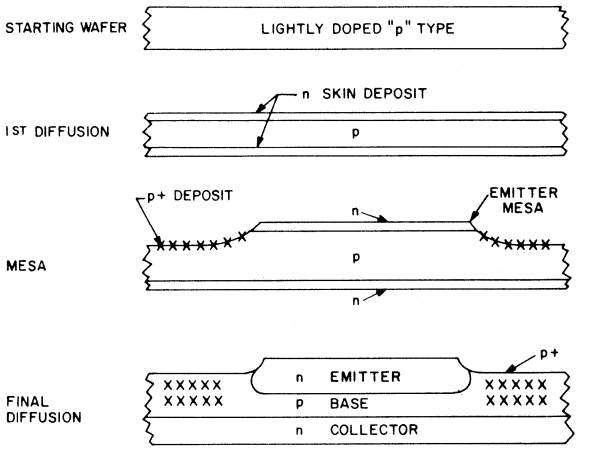


Fig. 9 – Processing steps in the manufacture of a hometaxial-base transistor.

development of a typical hometaxial-base transistor, and Fig. 10 shows a typical cross section of a completed single-diffused hometaxial transistor.

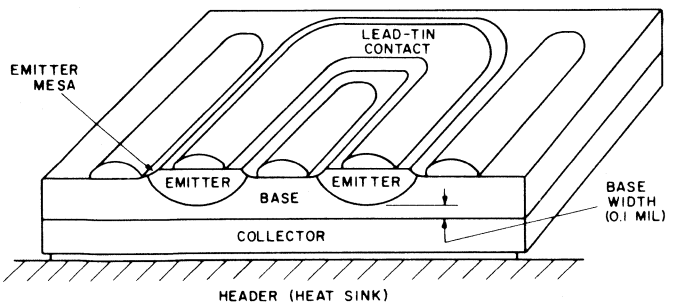


Fig. 10 – Hometaxial-base (single-diffused) transistor structure.

The chief advantages of the hometaxial-base transistors are good voltage ratings and excellent electronic ruggedness that permit these transistors to withstand repeated high-energy power pulses. Both advantages result from the very deep graded junctions and the wide base region. The graded junction provides a benefit of either higher voltage ratings with good saturation resistances, or much lower saturation resistances at a given voltage. The electronic ruggedness arises from the moderately wide, undiffused (homogeneous) base region which allows injected charge carriers to fan out and thereby reduce charge-carrier density at the collector junction where heating effects predominate. Another advantage is that the manufacturing cost per unit of power-handling capability is relatively low, primarily as a result of large-batch processing.

Hometaxial-base transistors have a relatively low switching-speed limit because of the moderately wide base spacing, and a low upper voltage limit of about 150 to 200 volts because of punch-through limitations.

Double-Diffused Transistors

Double-diffused transistors start with a relatively high-resistivity silicon wafer on which base dopant impurity is deposited. This dopant is then diffused to shallow depths. Then, an oxide (SiO_2) is selectively etched to define regions where an emitter impurity is to be deposited and diffused. The oxide acts as an effective mask against the diffusion of most of the usual impurity elements, such as boron or phosphorus. The emitter diffuses more rapidly than the base and, therefore, provides a means to narrow the base width until the desired electrical properties are obtained. The more rapid emitter diffusion results from a much higher impurity level, which enhances the diffusion coefficient as compared to that of the base diffusion. Fig. 11 shows a cross section of a typical double-diffused transistor.

The double-diffused structure differs from other designs in that the high-resistivity side of the collector-base junction

is on the collector side; therefore, the collector voltage can be designed almost independent of the base width. The advantage of the double-diffused transistor is that very narrow non-homogeneous or graded base widths are employed; the frequency responses of these devices, therefore, are orders of magnitude greater than those of earlier types of

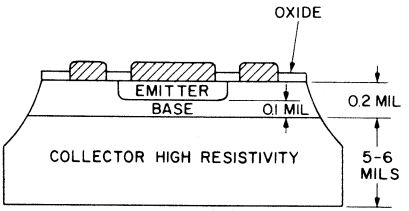


Fig. 11 – Double-diffused transistor structure.

transistors. Double-diffused transistors, however, have a very high collector saturation resistance and relatively fragile junctions because of the thick high-resistivity collector and narrow graded base width.

Double-Diffused Planar Transistors

The double-diffused planar transistor is essentially identical to the double-diffused type with one modification in the planar collector-base junction. The manufacturing process for the double-diffused planar transistor is similar to that for the double-diffused transistor, with the additional selective masking step for the base impurity. (An oxide similar to the emitter masking step is also used for this mask.) As shown in Fig. 12, the junction terminates at the surface of the silicon

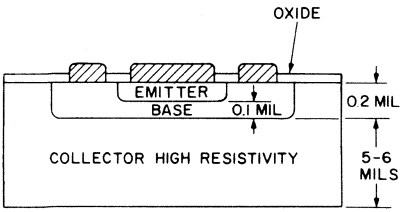


Fig. 12 – Double-diffused planar transistor structure.

wafer instead of on the side. The junction also terminates under a protective oxide layer.

The double-diffused planar transistor features drastically reduced collector leakage currents and better uniformity of device characteristics. The double-diffused planar structure allows the transistor to come very close to the low theoretical limit for silicon junction leakage current.

The disadvantages are similar to those of the double-diffused transistor, in that the double-diffused planar type has a very high collector saturation resistance and relatively fragile junctions. The double-diffused planar transistor has a collector voltage 10 to 20 per cent lower than that of mesa types with the same junction design.

Triple-Diffused Transistors

The triple-diffused structure is essentially identical to the double-diffused design except that a third diffusion is performed. The third diffusion, on the opposite side of the silicon wafer, eliminates the major disadvantage of the double-diffused design – high saturation resistance. In the triple-diffused transistor the wafer of silicon is coated with a dopant, followed by a controlled diffusion. Fig. 13 shows a typical cross section of a triple-diffused transistor.

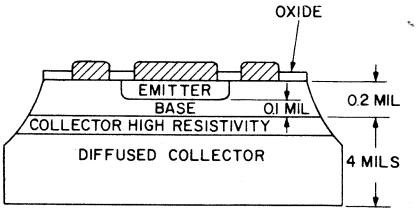


Fig. 13 – Triple-diffused transistor structure.

The principal advantage of the triple-diffused structure is that it has low saturation resistance which is of crucial importance in power transistor applications. The saturated switching speeds of this type of transistor are faster than

those of the double-diffused design. Both advantages are a result of the thinning down of the high-resistivity section while the bulk of the collector is heavily doped and highly conductive. This technique, however, results in relatively fragile junctions.

Triple-Diffused Planar Transistors

The triple-diffused planar transistor, which is similar in structure to the triple-diffused transistor, incorporates a planar collector, as shown in Fig. 14. Critical cross sections of

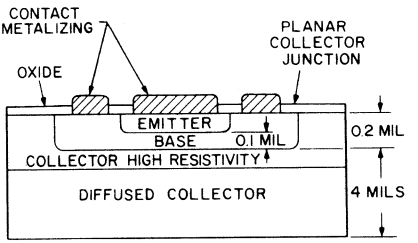


Fig. 14 – Triple-diffused planar transistor structure.

different stages of the manufacturing processes are shown in Fig. 15.

The principal advantages of the triple-diffused planar transistor are very low leakage current, high-speed operation, and low saturation resistance. The main disadvantage is that the cost of manufacturing is higher than that of non-planar devices.

Double-Diffused Epitaxial Transistors

The double-diffused epitaxial structure is similar in appearance to the triple-diffused design, except that the diffused collector region is replaced by a heavily doped homogeneous layer referred to as the epitaxial substrate. Because of the difference in doping between the double-diffused epitaxial and triple-diffused structures, some improvements in switching speeds and saturation resistance can be realized. The double-diffused structure, however, has a

somewhat poorer reverse "energy profile", so that its capability to withstand inductive or capacitive energy pulses is reduced.

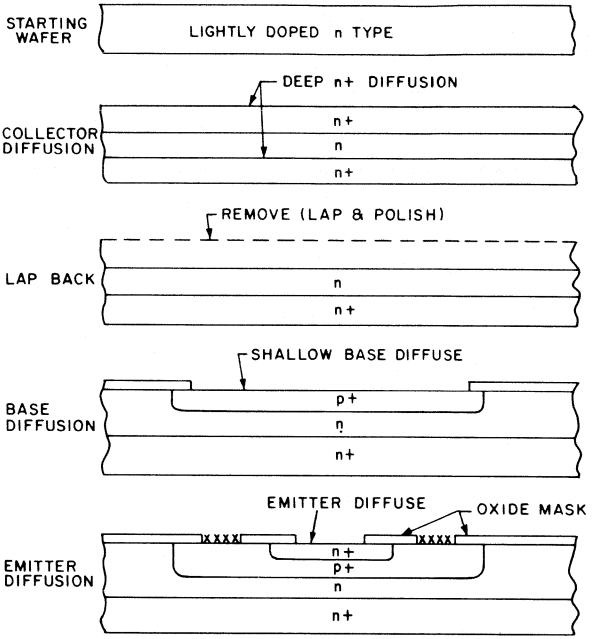


Fig. 15 — Processing steps in the manufacture of a triple-diffused planar transistor.

Fig. 16 shows a cross section of a typical double-diffused epitaxial transistor, and Fig. 17 shows a planar version of the same kind of transistor.

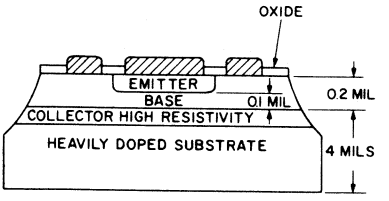


Fig. 16 — Double-diffused epitaxial transistor structure.

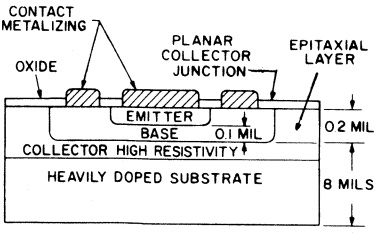


Fig. 17 — Double-diffused epitaxial planar transistor structure.

Epitaxial-Base Transistors

The epitaxial-base structure uses epitaxial layers in the actual formation of the base-collector junction. A single diffusion of the emitter completes this relatively simple design. A layer of impurity (opposite to the substrate impurity) is epitaxially grown on the highly doped substrate. An oxide masking and emitter diffusion into this epitaxial layer completes the construction. Fig. 18 shows a typical cross section of an epitaxial-base power transistor.

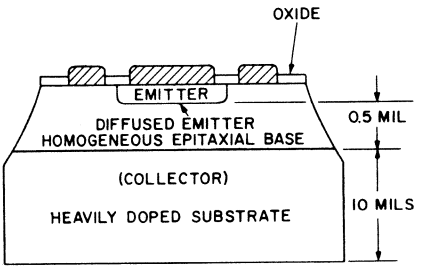


Fig. 18 – Epitaxial-base transistor structure.

The principal advantage of the epitaxial-base structure, compared to the double-diffused designs, is that it is electronically more rugged (able to withstand energy pulses) as a result of the wider and homogeneous base region. In comparison to the hometaxial structure, the epitaxial-base type has significantly higher frequency response and the ability to carry higher currents for an equivalent emitter area.

The disadvantage of the epitaxial-base design is that it is limited by low voltage ratings imposed by the constraint of the abrupt base-collector junction formed between the heavily doped collector substrate and the epitaxially deposited base layer. The low voltage rating also results from the thin base width necessary for adequate current gain which reduces voltage limits because of punch-through effects. The epitaxial-base transistor also suffers from moderate collector leakage-current levels resulting from step junctions and mesa construction.

Multiple-Epitaxial-Base Transistors

The multiple-epitaxial-base structure is similar to the epitaxial-base transistor, but has the added feature of a high-resistivity epitaxial layer for the active collector region. The multiple epitaxial-base transistor is fabricated from a heavily doped silicon wafer on which alternate layers of p-n or n-p high-resistivity silicon are epitaxially grown to create a π - ν or a ν - π base-collector junction. An emitter area is then diffused into the structure. Fig. 19 shows the various

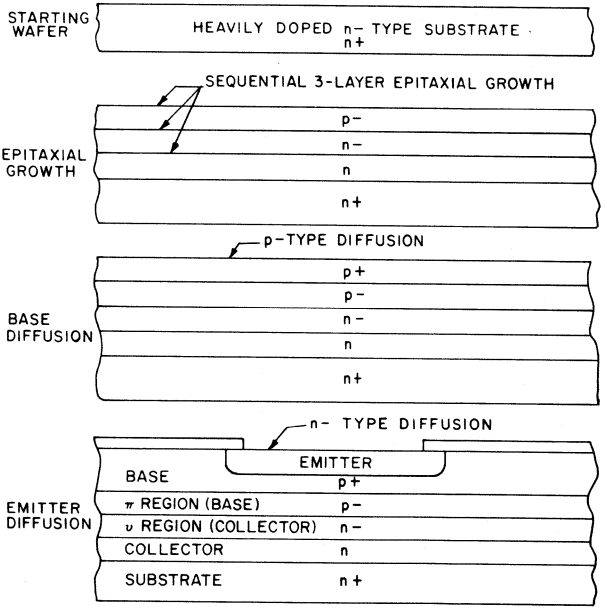


Fig. 19 — Processing steps in the manufacture of a multiple-epitaxial-base transistor.

stages in the manufacture of the multiple-epitaxial-base transistor structure, and Fig. 20 shows a typical cross section of this type of device.

The principal advantage of the multiple-epitaxial-base structure is that it has high voltage ratings with good current carrying abilities and excellent power-handling capabilities at

high voltages (second breakdown). The higher voltage ratings result because the transistor uses both the base and the collector regions to support the applied collector voltage. The good current-handling characteristic results from the fact that lower collector resistivity can be used for equivalent voltage ratings, as compared to double-diffused epitaxial designs. The lower collector resistivity also minimizes high-current fall-off effects that result from base widening. The excellent second breakdown characteristic results from the moderately wide base width and partial homogeneous base doping, which allows more charge-carrier fan-out (diffusion) and reduced current densities at the collector junction where heating effects predominate.

The principal disadvantage is that the cost of manufacturing the multiple epitaxial-base transistor is relatively high.

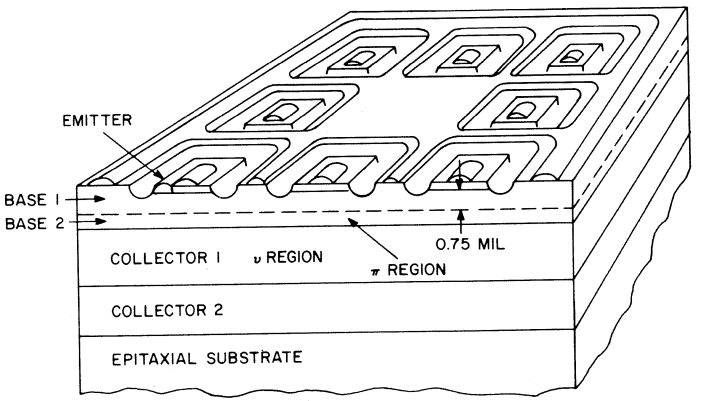


Fig. 20 – Multiple-epitaxial-base transistor structure.

Multiple-Epitaxial Double-Diffused Transistors

The multiple epitaxial double-diffused structure is almost identical to the double-diffused epitaxial design, with the exception that multiple epitaxial layers are used in the collector region, instead of a single collector layer. The top collector layer is a thin, high-resistivity layer followed by one or more thin, but more heavily doped, layers. These more

heavily doped layers are grown sequentially in an epitaxial system onto a thick, heavily doped silicon substrate wafer. Fig. 21 shows the various stages in manufacture of the multiple epitaxial double-diffused structure, and Fig. 22 shows a typical cross section of the completed transistor.

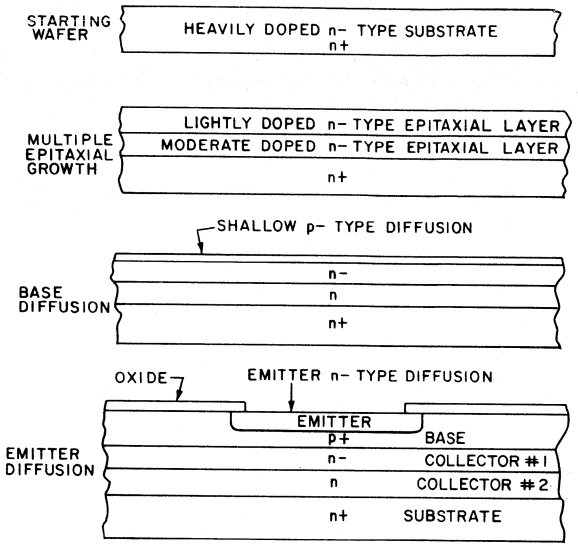


Fig. 21 — Processing steps in the manufacture of a multiple-epitaxial double-diffused transistor.

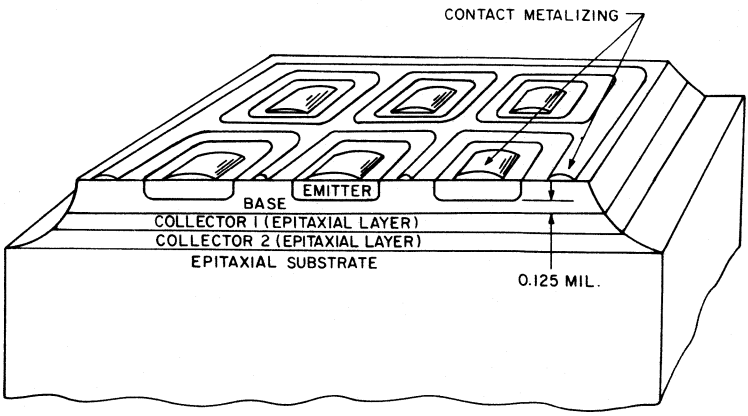


Fig. 22 — Multiple-epitaxial double-diffused transistor structure.

The advantages of the multiple epitaxial double-diffused structure include those of the double-diffused epitaxial design (high speed and low saturation), as well as the significant advantages of higher collector-junction voltage ratings, and increased electrical ruggedness. The electrical ruggedness (supplied by the additional collector layers) becomes even more of a factor during power switching with inductive loads in the 100-to-200-volt range where significant inductive energies (reverse second breakdown) may have to be handled by the transistor.

The disadvantages of the multiple epitaxial double-diffused transistor are the moderate-to-high cost per unit and the moderate leakage in the structure.

GEOMETRIES

The topography of a transistor is referred to as its geometry. This transistor geometry, in conjunction with its structure, establishes most of the fundamental transistor electrical, thermal, and economic properties. Proper geometric design of a transistor allows for many compromises, which may result in a variety of advantages and disadvantages from different structures.

The basic premise for most geometry designs for power transistors is to increase current handling per unit area of device. This condition results in lower-cost designs or, as in high-frequency transistors, higher-speed operation as a result of the smaller device areas.

Power-transistor geometries have evolved from the very early inefficient "ring-dot" configurations to the present-day sophisticated "overlay" concepts. Fig. 23 shows some typical geometry milestones in this evolutionary cycle.

The early geometries were characterized by simple shapes, large dimensional tolerances, and poor utilization of active regions. As the state of the art in fine-line mask making and wafer printing improved, the geometries became more involved, with much finer dimensions.

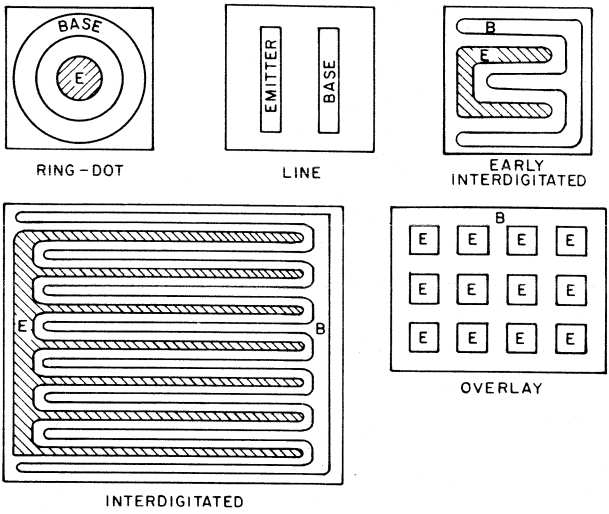


Fig. 23 – Typical geometries in the development of transistors.

In silicon power transistors, current crowding is the greatest contributor to reductions in current gain. Emitter periphery is the crucial design factor to reduce high current density caused by current crowding. Modern technology, however, has produced the means to yield more than 10 inches of periphery in less than 0.050 square inch of surface area.

Certain device structures have constraints on how fine the emitter geometry can be made. Refinement of emitters is governed by the space needed for emitter and collector mesas and by the thickness of oxide masks needed for deep diffusions, as well as by other factors. Table II shows progressive geometry refinements of some power-transistor structures.

PACKAGING

Three basic operations are involved in the packaging of a transistor pellet into a suitable package. These operations include: (1) attachment of the transistor pellet to the

package, (2) connection of the transistor emitter and base contact to the external leads of the package, and (3) formation of the metal-ohmic transistor contacts.

Table II - Geometry Refinements

Structure	Smallest Practical Emitter Width (nominal) mils	Emitter Mask Tolerance mils
Alloy	25	±3
Hometaxial-base	10	±1
Triple-diffused mesa (deep junctions)	2	±0.3
Double-diffused epitaxial planar (shallow junctions)	0.1	±0.01

Pellet Attachement

Three technologies predominate for attachment of transistor pellets to the transistor package. Soft solder, hard solder, or polymer adhesive may be used. Soft-solder and hard-solder methods are used almost exclusively for transistors designed to operate at power levels greater than one watt. The three approaches with their advantages and disadvantages are shown in Table III. Fig. 24 shows cross

Table III - Attachment Methods

Attachment Method	Materials	Advantages	Disadvantages
Soft solder	Lead-tin	Low cost, high-dissipation capability,	Can be fatigue prone
Hard solder	Gold-silicon	High-dissipation capability, strong	High attachment cost for large chips, needs molybdenum block
Polymer adhesive	Filled epoxies	Low cost	Poor thermal properties

sections for soft- and hard-solder methods of pellet attachment.

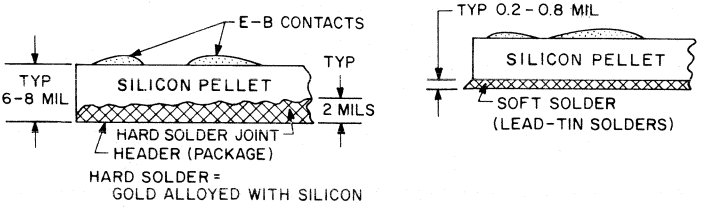


Fig. 24 — Pellet-attachment methods.

Lead Attachment

Two general methods encompass the technologies used for connecting the ohmic portion of the transistor pellet emitter and base contacts to the external leads of the package: wires (bonds) and soldered contacts (clips). Table IV shows the broad range of connections used for power

Table IV - Methods of Lead Attachment

Lead Connection	Method of Attachment	Materials Used	Advantages	Disadvantages
Thermo-compression bond	High temperature and pressure	Gold-wire ribbon	Very small areas	Costly in large devices
Nailhead bond	High temperature and pressure	Gold wire with end balled	Stronger than thermo-compression bond, less costly	Larger contact area required
Ultrasonic bond	Ultrasonic weld	Aluminum or gold wire	Avoid gold-alum. problems	Costly in large devices
Wire solder	Insert wire in molten solder	Suitable solderable wires	Moderate cost	Large contact area required
Clip solder	Pre-set into clips solder	Phosphor-bronze or nickel	Low cost	Large contact areas required

ransistors with some of their advantages and disadvantages. ?ig. 25 shows cross sections that illustrate the two methods)f lead connection.

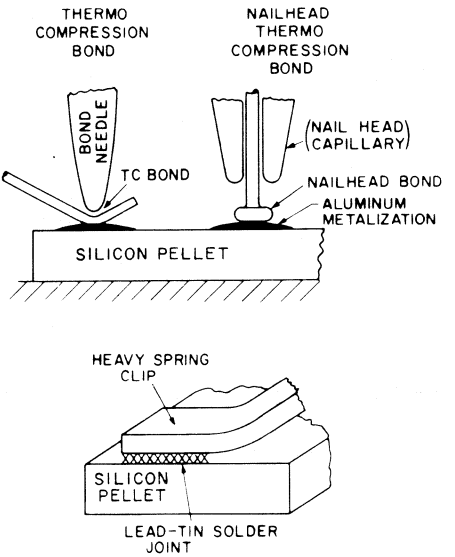


Fig. 25 – Two general methods of lead attachment.

Metal-Ohmic Contacts

The principal metal-semiconductor contact technology is divided into the following two categories: evaporated-and-alloyed metals and plated-and-sintered metals.

The evaporated-and-alloyed metals consist of aluminum, gold, and silver. Aluminum is used in almost all present designs because of its case of evaporation and alloying to the semiconductor, relative stability, and good metallurgical strength after wire bonding.

The plated-and-sintered contacts are used when large, heavy solder-coated contacts are needed. Large batch-plating and heat-treating (sintering) processes make these contacts very desirable for low-cost devices. Fig. 26 shows typical evaporated and plated techniques.

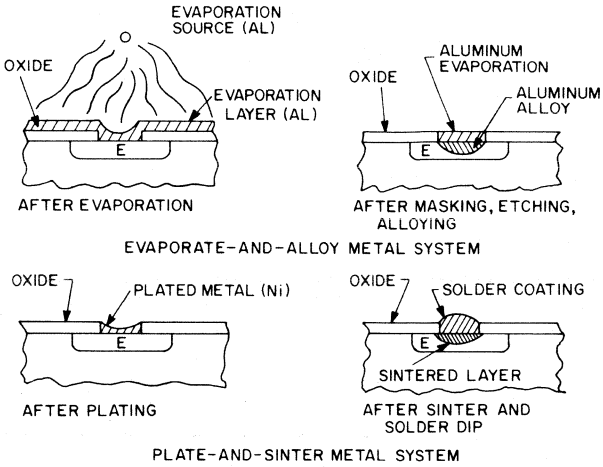


Fig. 26 — Typical evaporated and plated semiconductor contacts.

Safe Operating Area

A number of factors such as second-breakdown and dissipation capabilities, current and voltage ratings, and temperature critically affect the performance of power power transistors in various circuit applications. These factors define a safe operating area that indicates the maximum voltage-current product that the transistor should be subjected to in a circuit for both steady-state and pulsed operation.

SECOND-BREAKDOWN CONSIDERATIONS

Second breakdown is a potentially destructive phenomenon that can occur in all power transistors within the maximum current and voltage ratings of the device. A simplified explanation is that localized thermal regeneration occurs, and the transistor exhibits a lower value of breakdown voltage, referred to as the "second breakdown". The lower value of voltage results from thermal generation of charge-carrier pairs (holes and electrons) at high localized temperatures which alter the conductivity of the semiconductor in that vicinity. This localized effect reduces the ability of the transistor to support the applied voltage. Fig. 27 shows qualitatively what happens under primary or secondary breakdown.

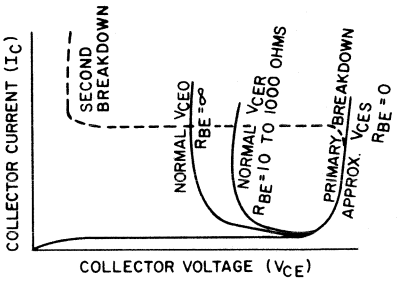


Fig. 27 – Primary and secondary breakdown voltages.

Reverse-Bias Second Breakdown

Reverse-bias second breakdown is a phenomenon that may occur when the collector current continues to flow under referse-bias conditions and causes the injected current to be concentrated in the central portions of the emitter, in contrast to the normal edge injection of the current. If the injected current is severely restricted to a very small central area by a large reverse emitter-base bias, the current density can rise to very large levels – in the order of thousands of amperes per square centimeter. If the collector of the transistor is of high-resistivity silicon, the high current density may inject a density of charge carriers that is equal to or greater than the collector impurity density. In this local region, the base widens and the collector depletion layer expands until the injected current density is smaller than the collector impurity density. If the current density is sufficiently high, the collector depletion layer expands to a more heavily doped collector region, such as an epitaxial substrate or a collector diffused region of a triple-diffused device. When the collector depletion layer expands, the collector breakdown voltage is governed by the impurity gradient related to the base doping and the heavily doped collector. The collector breakdown voltage normally supports only a fraction of the original voltage, and the second breakdown voltage results. The thermal effects from the large current densities also contribute to the regeneration process. Fig. 28 shows the process of reverse-bias second breakdown.

In an inductive circuit, a situation exists such that collector current flows in the forward direction while the transistor is being turned off, and a high voltage is induced across the device. As a result, the transistor enters the

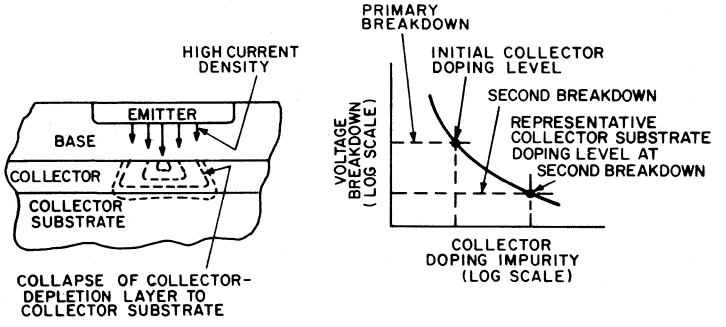


Fig. 28 – Reverse-bias second breakdown.

sustaining region. The hot spot that forms during reverse-bias second breakdown may then be generated by current crowding in the depletion region, as shown in Fig. 29.

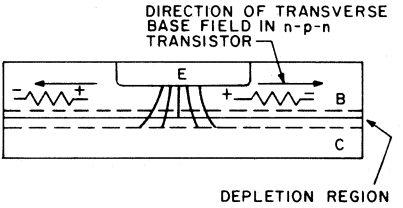


Fig. 29 – Cross section showing current crowding that occurs during reverse-bias second breakdown.

Device Conditions – The reverse base current that flows laterally through the base region creates an electric field. For an n-p-n transistor, electrons flow from the emitter to the collector across the base region. The field causes these carriers to flow mainly from the center of the emitter, because the emitter-base forward bias is greatest at this point. Because the device is in the sustaining region as a result of circuit conditions, a depletion region is present. Carriers

(electrons) that flow across this region, which resembles two plates of a capacitor, decrease in potential. Therefore, energy is transformed to heat and causes a hot spot and possibly reverse-bias second breakdown ($E_{S/b}$). Typical examples of this situation are circuits, such as those shown in Fig. 30, in which an unclamped inductive load or a non-commutated leakage inductance is present.

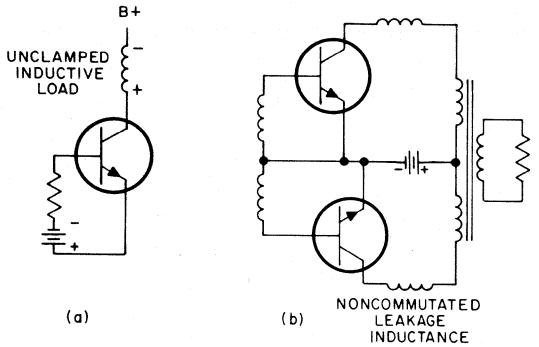


Fig. 30 – Examples of (a) unclamped inductive loads and (b) uncommutated leakage inductance.

Circuit Variables – Anything that increases the transverse base field aggravates hot-spot formation. Therefore, higher reverse base currents that result from decreased base-drive resistance or higher reverse voltages diminish $E_{S/b}$ capability, as shown in Fig. 31. This figure shows the effect of variations

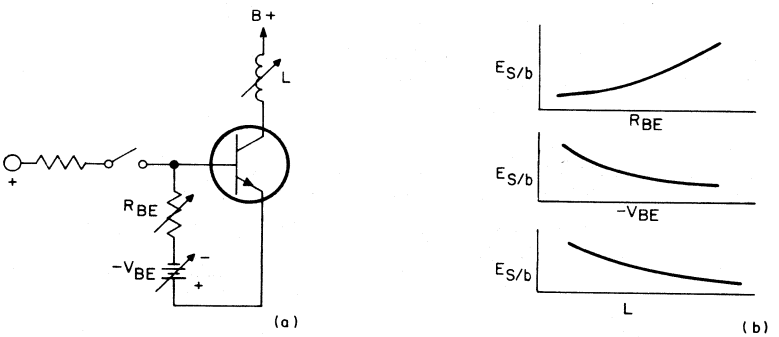


Fig. 31 – (a) Typical inductive-load circuit and (b) variation of second-breakdown capability as a function of circuit parameters.

in the external base-to-emitter resistance R_{BE}, the reverse base-to-emitter voltage $-V_{BE}$, and the load inductance L.

Test Facilities – A test set which makes the measurement of reverse-bias second breakdown possible and also protects the transistor being tested is shown in Fig. 32. A test cycle includes the following steps:

1. The transistor is driven to the desired collector-current level in saturation.

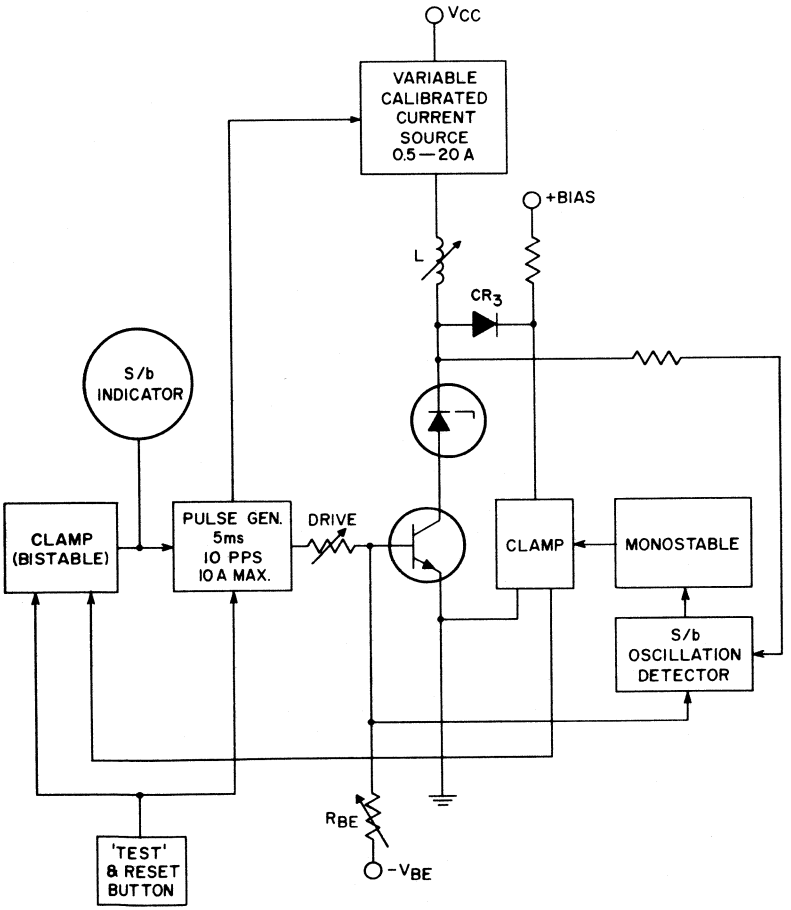


Fig. 32 – Reverse-bias second-breakdown ($E_{S/b}$) test set.

2. The transistor is reverse-biased.
3. The transistor enters the sustaining region, $V_{CEX}(sus)$.
4. Energy is absorbed by the transistor.

If failure occurs, high-frequency noise is sensed at the base of the transistor. A "crowbar" (transistor) in parallel with the transistor being tested is then turned on, and energy is shunted through this "crowbar" to protect the transistor undergoing the test. Fig. 33 shows the voltage-current relationship during the reverse-bias second-breakdown ($E_{S/b}$) test.

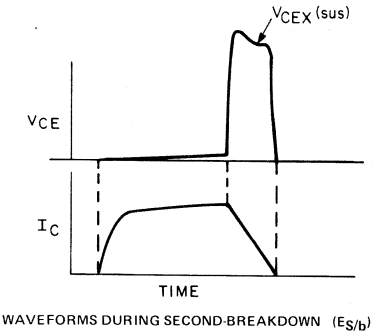


Fig. 33 – Waveforms during second-breakdown ($E_{S/b}$) test.

Forward-Bias Second Breakdown

Forward-bias second breakdown is somewhat different from reverse-bias second breakdown. As shown in Fig. 34, the localized heating results because the current density J

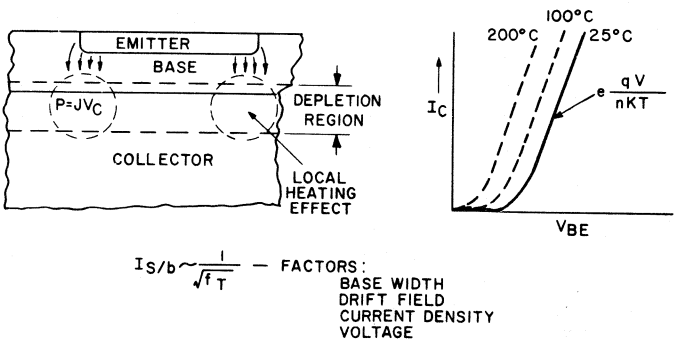


Fig. 34 – Forward-bias second breakdown.

crosses the depletion region (collector field) V_C to yield a power density P. As P increases, more current is injected into the localized area. The increase in current is caused by a decrease in the localized V_{BE}, at an approximate rate of 2 millivolts per °C. The local system becomes regenerative as more heat from the increased power density reduces V_{BE} and thereby increases the current injection.

Causes of Forward-Bias Second Breakdown – The forward-bias second-breakdown current, $I_{S/b}$, is defined as the current at the onset of second breakdown, and is closely related to the collector field V_C, the current density J, and other properties of the transistor. Forward-bias second breakdown is also related to charge-carrier transit time across the base region, and is controlled by base width and any accelerating fields that exist in the base. The longer the transit time required for the charge carrier to cross the base, the more lateral diffusion of the charge and thus the greater the reduction in the current density at the edge of the collector depletion layer. This diffusion effect, referred to as "fan-out," is enhanced by wide base widths and homogeneously doped bases. Because the forward-bias second breakdown is related to the base width, it is also related to frequency response. For a given structure, this frequency relationship is expressed by the following empirical equation:

$$I_{S/b} \approx \left(\frac{1}{\sqrt{f_T}}\right)K$$

Operation in the forward-bias region subjects the transistor to simultaneous current and voltage. This condition causes current concentrations as previously discussed. This type of rating must be considered for all linear applications of transistors.

Forward-Bias Second-Breakdown Current Test Set – The block diagram of a nondestructive second-breakdown test set is shown in Fig. 35. The transistor under test is in series with a pass transistor and is driven by a differential amplifier at a current level selected by the operator. The level selected is

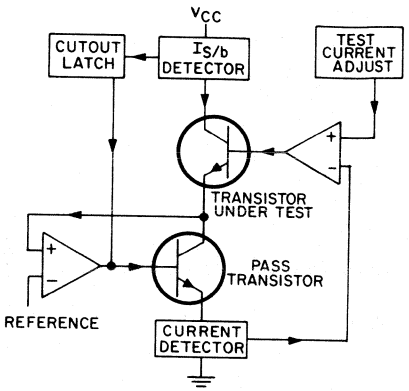


Fig. 35 — Block diagram of test set for forward-bias second-breakdown current ($I_{S/b}$).

independent of transistor current transfer ratio. The pass transistor is operated out of saturation, so that fast turn-off is possible. A second differential amplifier senses the voltage across the pass transistor and the 1-ohm resistor in series with it. This voltage is held constant throughout the test to improve the accuracy of the second-breakdown-voltage reading. The circuit is arranged so that only the collector current of the transistor under test passes through the 1-ohm resistor. The voltage across this resistor, therefore, provides an accurate indication of collector current.

The onset of second breakdown is detected by use of the primary of a pulse transformer connected in series with the collector of the transistor under test. Under second-breakdown conditions, the rapid rate of rise of collector current induces a voltage L(di/dt) in the transformer secondary which is coupled to the input circuit of the series pass transistor. This voltage turns off the series pass transistor in one microsecond. Simultaneously, a voltage is developed across the transformer primary of a polarity that immediately reduces the voltage across the transistor under test. The inductance of the transformer also aids in limiting immediate current rise in the transistor being tested.

The test-set characteristics, together with the protective cutout circuit, prevent damage to the transistor during the second-breakdown test. The complete cutout time of the actual test set is approximately one microsecond; this value is sufficient to prevent destruction of any transistor currently available.

The pulse width of the voltage and current applied to the transistor under test can be varied from 0.5 millisecond to several seconds. For dc second-breakdown tests, a pulse width of 0.5 to 2 seconds is required because the thermal time constant of the power-transistor pellet and mounting block may be several tenths of a second.

A comparison of energy-handling capability for several transistor structures is shown in Table V.

Table V - Comparison of Energy-Handling Capability

		$I_C \times V_{CEO}$ (1-Second pulse)	Forward Bias Energy Handling at V_{CEO} Limit J	Reverse-Bias Energy $E_{S/b}$ mJ
Complementary Doped - $\pi\nu$	TA7007	0.2 x 300	60	23
	TA7402	0.5 x 300	150	150
	2N5240	0.08 x 300	24	1.6
	2N5840	0.02 x 350	7.0	0.45
Double-diffused, double-epitaxial	2N5038	0.25 x 90	22.5	13
	2N5672	0.12 x 120	14.4	20
	2N6032	0.05 x 120	6	40
	2N3879	0.09 x 75	6.85	1.0
Triple-diffused	2N5805	0.10 x 300	30	0.62
	2N3585	0.03 x 300	9	0.05
Hometaxial-Base	2N5578	1.5 x 70	105	800
	2N3055	1.9 x 60	115	170
	2N3773	0.6 x 140	84	310

INDUCTIVE VOLTAGE-BREAKDOWN TESTING

In most practical applications of transistors, the highest voltage that appears across the transistor results from the

turn-off of the transistor, because the transistor switches from a high-current "on" state to a "cut-off" state. Inductive testing simulates this condition very closely, as shown in Fig. 36. Curve-tracer testing, on the other hand, subjects the transistor to an increasing voltage until the required current is

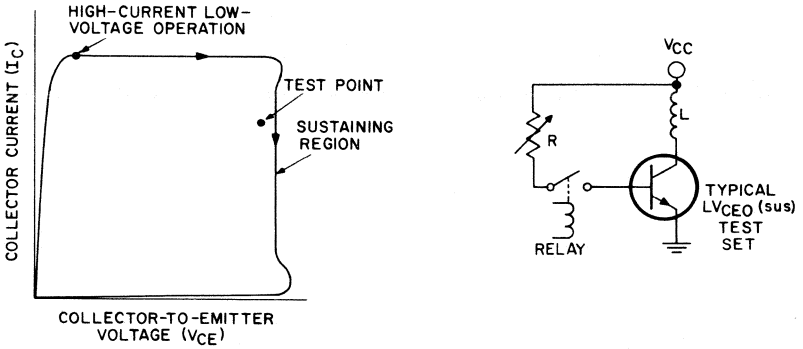


Fig. 36 — Inductive voltage-breakdown testing of a transistor: (a) load line; (b) test circuit.

achieved; i.e., the high-current, high-voltage measuring point is approached from the other direction with the collector current I_C lagging the collector-to-emitter voltage V_{CE}, as shown in Fig. 37. Unless sufficient current is supplied to place the transistor in the sustaining region, the breakdown voltage measured is artificially high. If this high current is passed through a transistor with a high breakdown voltage, a high dissipation results. This dissipation is not uniformly distributed over the whole junction, but tends to concentrate in the spots with the lowest breakdown. This concentration is

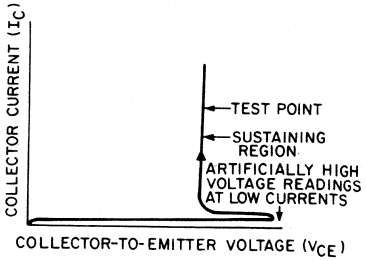


Fig. 37 — Load line for curve-tracer voltage-breakdown testing.

further aggravated when the base-to-emitter junction is reverse-biased. The small areas that break down first form hot spots. These hot spots result in further current concentration with time, and possible device destruction. Fig. 38 shows the test circuit used in the curve-tracer test.

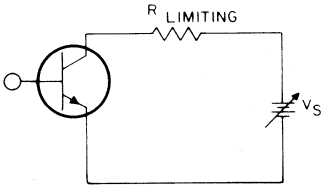


Fig. 38 – Test setup for curve-tracer voltage-breakdown testing.

The 8-millisecond sweep of a curve tracer is relatively slow compared to inductive sweeping. This sweep allows time for the current to concentrate and to deliver an appreciable and variable amount of energy. Inductive testing, on the other hand, delivers a relatively fixed amount of energy in a short time (0.6 millisecond maximum for the 2N4348 transistor). Less concentration of current is allowed, and the test is potentially less destructive and provides a more realistic rating. Curve-tracer testing may reject transistors that will operate satisfactorily in any practical application because the opportunity for the occurrence of hot spots is increased, and lower values of V_{CEO} are measured.

EFFECT OF TEMPERATURE ON SILICON TRANSISTORS

The characteristics of transistors vary with changes in temperature. In view of the fact that most circuits operate over a wide range of environments, a good circuit design should compensate for such changes so that operation is not adversely affected by the temperature dependence of the transistors.

Current Gain

The effect of temperature on the gain of a silicon transistor is dependent upon the level of the collector

current, as shown in Fig. 39. At the lower current levels, the current-gain parameter h_{FE} increases with temperature. At higher currents, however, h_{FE} may increase or decrease with a rise in temperature because it is a complex function of many components.

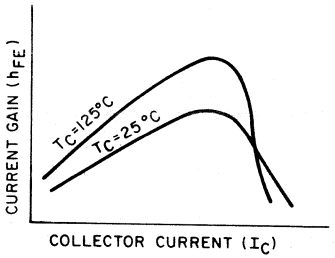


Fig. 39 – Current gain as a function of collector current at different temperatures.

Base-to-Emitter Voltage

Fig. 40 shows the effect of changes in temperature on the base-to-emitter voltage (V_{BE}) of silicon transistors. Two factors, the base resistance ($r_{bb'}$) and the height of the potential barrier at the base-emitter junction ($V_{BE'}$), influence the behavior of the base-to-emitter voltage. As the

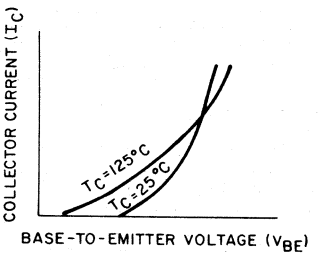


Fig. 40 – Collector current as a function of base-to-emitter voltage at different temperatures.

temperature rises, material resistivity increases; as a result, the value of the base resistance $r_{bb'}$ becomes greater. The barrier potential $V_{BE'}$ of the base-emitter junction, however, decreases with temperature. The following equation shows the relationship between the base-to-emitter voltage and the two temperature-dependent factors:

$$V_{BE} = I_B r_{bb'} + V_{BE'}$$

$$= \frac{I_C}{h_{FE}} r_{bb'} + V_{BE'}$$

As indicated by this equation, the base-to-emitter voltage diminishes with a rise in temperature for low values of collector current, but tends to increase with a rise in temperature for higher values of collector current.

Collector-to-Emitter Saturation Voltage

The collector-to-emitter saturation voltage $V_{CE}(sat)$ is affected primarily by collector resistivity (ρ_C) and the amount by which the natural gain of the device (h_{FE}) exceeds the gain with which the circuit drives the device into saturation. This latter gain is known as the forced gain (h_{FEf}).

At lower collector currents, the natural h_{FE} of a transistor increases with temperature, and the IR drop in the transistor is small. The collector-to-emitter saturation voltage, therefore, diminishes with increasing temperature if the circuit continues to maintain the same forced gain. At higher collector currents, however, the IR drop increases, and gain may decrease. This decrease in gain causes the collector-to-emitter saturation voltage to increase and possibly to exceed the room-temperature (25°C) value. Fig. 41 shows the effect of temperature on the collector-to-emitter saturation voltage.

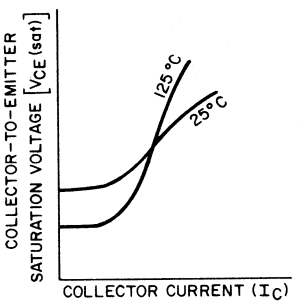


Fig. 41 — Collector current as a function of collector-to-emitter saturation voltage at different temperatures.

Collector Leakage Currents

Reverse collector current is a resultant of three components, as shown by the following equation:

$$I_R = I_D + I_G + I_S$$

Fig. 42 shows the variations of these components with temperature.

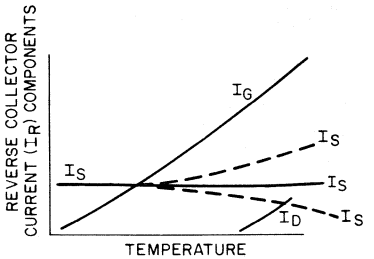


Fig. 42 — Reverse collector current as a function of temperature.

The diffusion or saturation current I_D is a result of carriers that diffuse to the collector-base junction and are accelerated across the depletion region. This component is small until temperatures near 175°C are reached. The component I_G results from charge-generated carriers that are created by the flow of diffusion carriers across the depletion region. This component increases rapidly with temperature. I_D and I_G are referred to as bulk leakages. The term I_S represents surface leakage which is caused by local inversion, channeling, ions, and moisture. This leakage component is dependent on many factors, and its variations with changes in temperature are difficult to predict.

At low temperatures, either surface or bulk leakage can be the dominant leakage factor, particularly in transistors that employ a mesa structure. At high temperatures, charge-generated carriers and diffusion current are the major causes of leakage in both mesa and planar transistor structures; the current I_G, therefore, is the dominant leakage

component. Because of the dominance of surface leakage I_S at low temperatures and the fact that this leakage may vary either directly or inversely with temperature, it is not possible to define a constant ratio of the leakage current at low temperatures to that at high temperatures. In view of the fact that power transistors are normally operated at high junction temperatures, it is more meaningful to compare the leakage characteristics of both mesa and planar transistors at high temperatures. The relative reliability of different types of power transistors, which is in no way related to the magnitude of low-temperature leakage current, is also best compared at high temperatures

PULSED SAFE-AREA SYSTEMS

On the basis of the heat storage in the thermal mass of the silicon chip and its mounting system, the peak power-handling capability of transistors increases with decreases in pulse duration. Fig. 43 shows normalized thermal resistance N_R as a function of time for a specific transistor and indicates that power substantially higher than rated steady-state values may be applied for short periods of time without exceeding the maximum rated junction temperature. These values of increased power correspond to

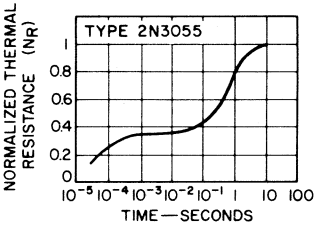


Fig. 43 – Normalized thermal resistance.

$(1/N_R)\ P_{(dc)}$, where $1/N_R$ is the normalized power multiplier and $P_{(dc)}$ is the steady-state power rating at the case temperature of interest.

The dissipation-limited region of the pulsed safe-area rating chart shown in Fig. 44 is prepared by use of the normalized thermal resistance from the following equation:

$$P_{diss} = [T_J(max) - T_C] / \theta_{J\text{-}C}(N_R)$$

This equation indicates a constant-power curve which can be represented on a log-log volt-ampere graph by a straight line that has a slope of -1 (from $I = PV^{-1}$).

The pulsed power curves are usually calculated and then verified by nondestructive tests along the constant-power curves from low to higher voltages. When dissipation is the only limiting factor, the -1 slope is continued to the transistor forward-biased avalanche breakdown voltage rating, at which point $Va_M = 1$ and may be approximated by

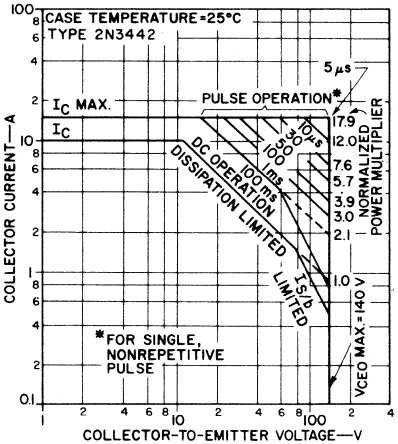


Fig. 44 — Safe-operating-area chart.

$V_{CEO}(sus)$. When second breakdown ($I_{S/b}$) is the limiting factor, the slope changes from -1 to a higher value, usually between -1.5 and -4, according to the following relationship:

$$I_{S/b} = PV^{-N}$$

Fig. 45 shows the derating curve for operation of a power transistor at case temperatures above 25°C. The $I_{S/b}$ limit is derated less with increasing temperature than the dissipation limit because the concentration of current that results in circuit breakdown is less severe than dissipation factors as temperature increases.

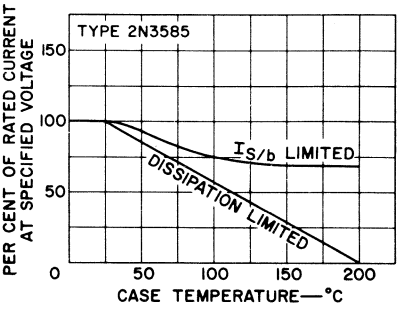


Fig. 45 – Derating curve for case temperatures above 25°C.

For pulsed operation, the derating factor shown in Fig. 45 must be applied to the appropriate curve on the safe-area rating chart. For the derating, the effective case temperature $T_C(eff)$ may be approximated by the average junction temperature $T_j(av)$. The average junction temperature is determined as follows:

$$T_j(av) = T_C + P_{AV}(\theta_{J\text{-}C})$$

This approach results in a conservative rating for the pulsed capability of the transistor. A more accurate determination can be made by computation of actual instantaneous junction temperatures. (For more detailed information on safe-area ratings and temperature derating the reader should refer to the manual, RCA Power Circuits, Technical Series SP-51, pp. 94 to 105 (RCA Electronic Components, Harrison, N. J.).

Depending upon whether time markers can be placed along the load line, two methods are available to determine whether a transistor will be operated within its safe-area limits in a given circuit.

1. Without Time Markers: The energy of the load line is concentrated at a single point (I_W, V_W) at which the greatest load-line penetration outside the safe area occurs. Multiplication of the waveforms of collector current I_C and the collector-to-emitter voltage V_{CE} yields a waveform of instantaneous power as a function of time. Integration of one

cycle of this instantaneous-power waveform results in an energy E. The width (t_p) of an equivalent pulse may be determined as follows:

$$t_p = E/V_W I_W$$

The voltage V_W, the current I_W, and the pulse width t_p are compared to the corresponding values of the pulsed safe area on the derated curves.

2. With Time Markers: If time-marked load lines are available, either through the use of dual-trace waveforms of collector-to-emitter voltage and collector current as a function of time or Z-axis modulation of oscilloscope traces, an alternative approach may be used. The marked load line is sketched on the derated curves. If the transistor is being operated in the safe area, the trace time of the portion of the load line that extends outside a given pulsed safe area should not be greater than the specified pulsed width for that safe area. For example, the load line should not spend more than 1 millisecond outside the 1-millisecond safe area.

Thermal Fatigue

Significant temperature variations occur in power transistors because of changes in ambient temperature and in the power dissipation during operation. These variations in temperature result in cyclic mechanical stresses at the interface of the semiconductor pellet and the metal header to which the pellet is bonded because of the difference in the thermal expansions of these parts. These stresses are a function of the difference in the coefficients of thermal expansion of the semiconductor and metallic materials, of the change in temperature at the interface, and of the dimensions of the interface.

TABLE VI

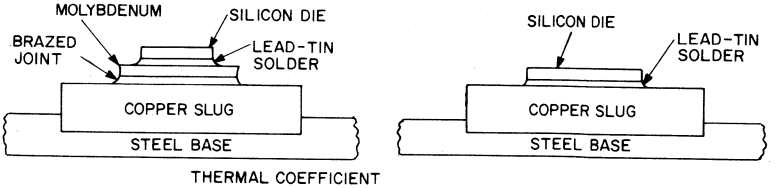
THERMAL-CYCLING REQUIREMENTS FOR TYPICAL APPLICATIONS OF POWER TRANSISTORS

Application	Circuit	P_T (W)	ΔT_C (°C)	Minimum Equipment Life Required (years)	Typical Thermal-Cycling Rating Required (cycles)
Auto radio audio output	Class A	8	75	5	5,000
	Class AB	2	45	5	5,000
Power supply	Series regulator	50	65	5	5,000
	Switching regulator	15	65	5	5,000
Hi-Fi audio amplifier	Class AB	35	50	5	5,000
Computer power supply	Series regulator	50	65	10	10,000
Computer peripheral equip.	Solenoid driver	5	5	10	1.3×10^8
Television	Vertical output	10	75	5	5,000
	Audio output	8	75	5	5,000
Sonar modulator	Linear amplifier	100	55	10	144×10^3

Power transistors are subjected to thermal-cycling stresses in all practical applications. Table VI lists examples of the thermal cycling that a power transistor may be required to withstand in several typical applications. These data show that the thermal-cycling requirements may be very severe even in some of the more common types of applications. The cyclic stresses produced by the continuous thermal cycling may result in dislocation "pile-ups" at points of discontinuity such as may be produced by voids and impurities. Such dislocations cause localized hardening and cracks that may eventually lead to transistor failures. This type of failure may be considered simply as fatigue wearout that results from continuous flexing of materials during thermal cycling.

IMPROVEMENT OF THERMAL-CYCLING CAPABILITY

The thermal-cycling stresses set up at the interface of two dissimilar materials because of the difference in the coefficients of thermal expansion of the materials can be reduced by insertion of a material that has an intermediate expansion coefficient between them. Fig. 46(a) illustrates the use of a molybdenum slab as an expansion matcher in a silicon power transistor to reduce the cyclic thermal stresses



MATERIAL	THERMAL COEFFICIENT OF EXPANSION X 10^{-6} PER °C
SILICON	4.2
MOLYBDENUM	4.9
COPPER	17.0
STEEL	11.0

(a) (b)

Fig.46 — Cross section of a transistor that uses a molybdenum expansion matcher between pellet and header; (b) cross section

between the silicon pellet and the copper header. Use of this technique can result in significant improvement in the thermal-cycling capability of power transistors.

Use of silicon-gold eutectic bonding to attach the semiconductor pellet to the header results in a pellet-to-header joint that can withstand a very large number of number of thermal cycles. When this type of hard-solder bonding is used, however, the stress generated because of a thermal mismatch is transmitted to the pellet, which in most power transistors is made of silicon. Because silicon is relatively weak in tensile strength and is highly "notch sensitive," the cyclic thermal stresses may result in the propagation of cracks in the silicon pellet unless either the pellet is very small or an expansion matcher is used.

In most silicon power transistors, lead solder is used to bond the pellet to the header. The cyclic thermal stresses produced at the mounting interface are then absorbed by non-elastic deformation of the soft solder material, and very little stress is transmitted to the pellet. The continuous flexing of the solder, however, may eventaually lead to fatigue failure in this material. Any impurities in the solder results in dislocation pile-ups that accelerate the failure. RCA has developed a process that significantly reduces the impurities introduced into the lead solder. Use of this proprietary "controlled solder process" (CSP) makes it possible to avoid microcracks that propagate to cause fatigue failures in power transistors and, therefore, greatly increases the thermal-cycling capability of these devices.

THERMAL-CYCLING RATING CHART

An equipment manufacturer should make certain that power-transistor circuits are designed so that cyclic thermal stresses are mild enough to assure that no transistor fatigue failures occur during the required operating life of this equipment. Experimental results indicate that the thermal-cycling capability of a power transistor can be predicted by use of the following mechanical-activation energy equation:

$$N = Ae^{\gamma_O/\Delta T}$$

where N is the number of cycles to failure, A is a system constant, γ_O is a constant proportional to the mechanical-activation energy required to produce a failure, and ΔT is proportional to the energy supplied as a result of the change in temperature at the mounting interface.

The above equation, together with empirical data, forms the basis for *a* new thermal-cycling rating system developed by RCA. This rating system, which is the first of this type in the industry, shows the relationship between total transistor power dissipation, the change in case temperature, and the number of thermal cycles that the transistor is rated to withstand.

Fig. 47 shows a typical thermal-cycling rating chart. This chart is provided in the form of a log-log presentation in which total transistor power dissipation is denoted by the ordinate and the thermal-cycling capability (number of cycles to failure) is indicated by the abscissa. Rating curves are shown for various magnitudes of change in case temperature. Use of this chart makes it possible for a circuit designer to avoid transistor thermal-fatigue failures during

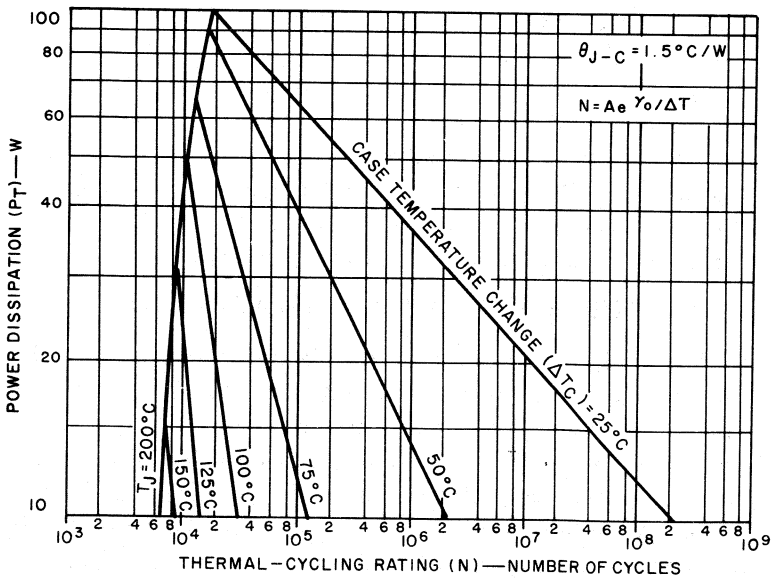


Fig. 47 — Typical series-regulator power supply.

the operating life of this equipment. In general, power dissipation is a fixed system requirement. The designer also knows the number of thermal cycles that a power transistor will be subjected to during the minimum required life of the equipment. For these conditions, the chart indicates the maximum allowable change in case temperature. (If the rating point does not lie exactly on one of the rating curves, the allowable change in case temperature can be approximated by linear interpolation.) The designer can then determine the minimum size of heat sink required to restrict the change in case temperature within this maximum value.

Thermal-cycling ratings are included in the technical data for all RCA silicon power transistor announced since January 1, 1971. Similar ratings are being added for earlier power transistors as soon as sufficient date are accumulated.

THERMAL-FATIGUE TESTING

The RCA thermal-cycling ratings allows a circuit designer to use power transistors with assurance that fatigue failures of these devices will not occur during the minimum required life of his equipment. These ratings provide valid indications of the thermal-cycling capability of power transistors for all types of operating conditions. On the basis of these ratings, limiting conditions can be established during circuit design so that the possibility of transistor thermal-fatigue failures are avoided.

Obviously, all individual power transistors cannot be tested to determine their thermal-cycling capability because such tests are expensive, time consuming, and destructive. The validity of the RCA thermal-cycling ratings results from the application of stringent process controls at each step in the manufacture of power transistors and from the testing of a statistically significant number of samples. Thermal-cycling ratings for power transistors provide the same type of assurance that a device will not fail when operated within ratings as that provided by the more familiar voltage, current, and second-breakdown ratings.

During thermal-fatigue testing of power transistors, the operating power for the device is usually equivalent to that expected to be applied during normal operation. The transistor is operated until the rise in case temperature is equal to the maximum value anticipated in the intended application. The case temperature is then reduced to the initial value by use of forced-air or water cooling. The cycle is repeated until failure occurs, as indicated by a significant increase in the transistor thermal resistance. The transistor heat sink and the timing of the temperature-cycling are selected to simulate as closely as possible the actual conditions that the transistor will be subjected to in the actual application. Table VII shows the results of thermal-fatigue tests on several RCA transistors.

Table VII - Thermal-Fatigue Performance of some Typical RCA Power Transistors

Type	Pellet Size Mils x Mils		Mounting Material	Material to which Die is Attached	CSP	Change in Case Temp. °C	Power Dissipation Watts	No. of Cycles to 10% Failure
2N3773*	250	250	Lead	Copper	No	42	85	1,000
2N3773	250	250	Lead	Molybdeum	No	42	85	9,600
2N3772	250	250	Lead	Copper	Yes	90	16	34,500**
2N3055	180	180	Lead	Copper	No	65	50	3,500
2N3055	180	180	Lead	Copper	Yes	90	6.7	40,000***
2N6032	230	230	Silicon Gold	Molybdeum	No	53	105	12,793***
2N5298	130	130	Lead	Copper	No	50	18	10,000
2N5240	130	130	Lead	Copper	Yes	42	51	8,500***
2N5039	145	183	Lead	Copper	Yes	73	59	10,000***

* Early design.

** Test still operating.

*** Test terminated—less than 10% failure.

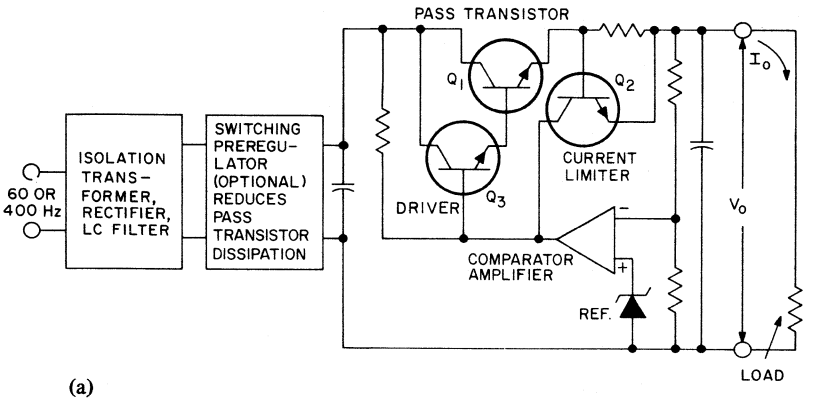
Applications

This section describes a number of representative applications of power transistors operated in both linear and switching modes. The requirements of the transistors in each type of application are explained, and their specific functions in various types of circuits are described. Important transistor characteristics for linear applications, such as safe operating area and power dissipation, are emphasized by examination of the operation of power transistors in series voltage regulators and linear power amplifiers. Important characteristics for switching applications, such as switching times and saturation voltages, are illustrated by examination of power-transistor operation in switching regulators, inverters, and converters.

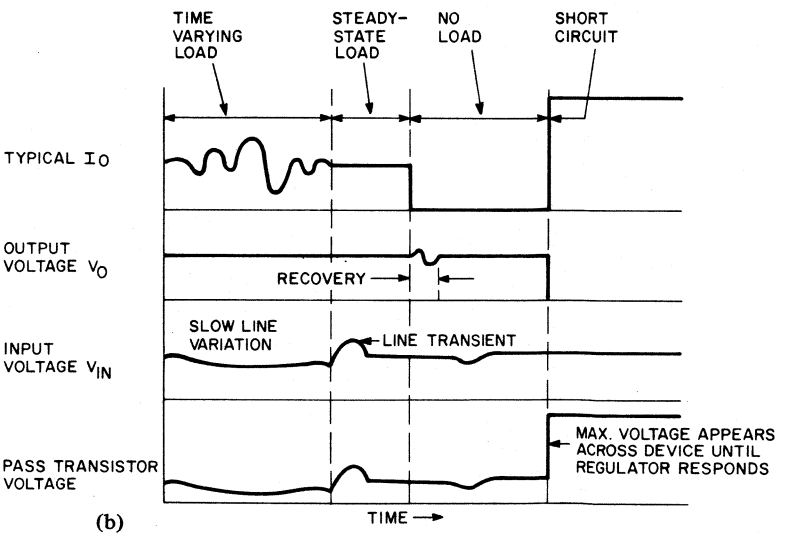
SERIES VOLTAGE REGULATOR

A series voltage regulator, such as that shown in Fig. 48(a), is so named because it is used in series with a power source and a load. The prime function of the series-regulator transistor, Q1, is to maintain a constant output voltage across the load, regardless of load or line variations. A current-limiter transistor, Q2, limits the series transistor so that the output current cannot exceed a rated maximum value, even in the event of a short circuit across the output terminals. The series pass transistor Q1, because of the rapid variation of the voltage across it, helps to filter out residual ripple voltages as supplied from the filter or preregulator. As

a result of the filtering action, the dc voltage that appears at the output terminals has an extremely small ripple component, as shown in Fig. 48(b). The switching preregulator. shown in Fig. 48(a), may be used to control the major portion of power to the load, and thus to reduce the power-dissipation requirements of the series-regulator circuit.



(a)



(b)

Fig.48 — Typical series-regulator power supply: (a) circuit diagram; (b) operating voltage and current waveforms.

Fig. 49 shows some typical load lines that indicate the major characteristics of the series-regulator pass-transistor application.

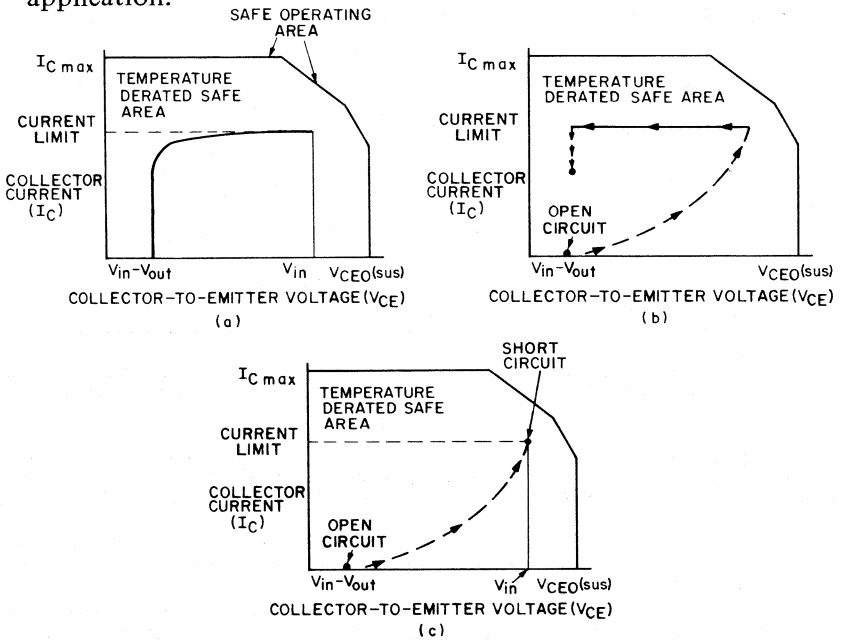


Fig. 49 – Typical load lines for series-regulator pass transistors: (a) load line for varying resistive load; (b) load line for RC load; (c) load line for applied short circuit.

The series-regulator circuit compares a fraction of the output voltage (as sampled by a resistive voltage divider) with a reference voltage. The pass transistor is driven by a current proportional to the difference between these two voltages. A negative feedback loop is formed so that if the output voltage V_O tends to decrease, the pass transistor is driven harder to increase V_O to its original value. If the response of the regulator to the compared voltages is fast enough, no excursions of V_O can be observed. Variations in the line voltage and voltage drift are filtered by the pass transistor, and V_O remains constant. If the load on the supply is suddenly removed, a slight overshoot of V_O may occur for a short length of time, known as the recovery time. This

overshoot may be decreased by connection of a capacitor of the correct value in parallel with the output. A sudden short circuit causes the load current I_O to be limited to the rated value of the supply, and the full filtered line voltage is applied across the pass transistor.

Some important characteristics of the series regulator are as follows:

1. The output voltage V_O remains constant during line-voltage and load-current variations. This feature is a function of the feedback-loop gain, including the dc current-transfer ratio h_{FE}.

2. The output voltage remains smooth during transient load changes. The smoothness of V_O is dependent upon the ac loop gain, including the h_{fe} of the pass transistor.

3. In case of a short circuit, the full input voltage appears across the pass transistor while the limit current flows through it. The second-breakdown collector current $I_{S/b}$ and the maximum collector-to-emitter voltage V_{CEO} of the transistor must be adequate to withstand this condition.

4. The highest output voltage obtainable is the filtered input voltage minus the collector-to-emitter voltage of the pass transistor. This voltage is dependent upon the circuitry used to drive Q1.

LINEAR AMPLIFIERS

A linear amplifier is designed to duplicate an input waveform as closely as possible, except that the output amplitude of the waveform is increased over that of the input. Linear amplifiers are usually divided into two categories -- Class A and Class B.

Class A

Class A amplifiers are usually used for linear service at low power levels. Fig. 50 shows a basic class A amplifier.

The maximum efficiency of a class A amplifier is 50 per cent; in practice, however, this efficiency is not realized. The class A transistor amplifier is usually biased so that the quiescent collector current is midway between the maximum and minimum values of the output-current swing. Collector current, therefore, flows at all times and imposes a constant drain on the power supply. The consistent drain is a distinct disadvantage when higher power levels are required or when operation from a battery is desired. Consequently, higher-power amplifiers are usually class B, push-pull types.

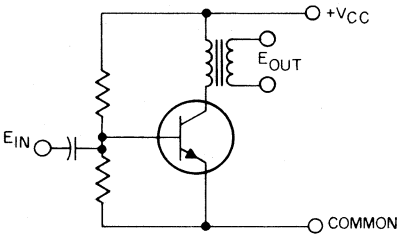


Fig. 50 – Basic class A transformer-coupled amplifier.

Class B

The class B, push-pull amplifier can be used for applications such as audio amplification, servo motor drives, or a yoke driver for magnetic deflection. This amplifier may also be used to modulate the supply voltage (B+) of rf amplifiers in order to generate an amplitude-modulated signal, or to drive sonar transducers for high-power undersea applications. Such amplifiers may be designed in several ways. One example, a push-pull quasi-complementary-symmetry amplifier, is shown in Fig. 51.

Some of the major characteristics of the audio amplifier are indicated by the typical operating waveforms and the

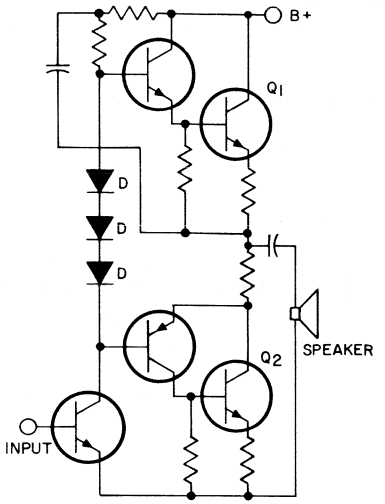


Fig. 51 – Class AB, push-pull quasi-complementary-symmetry amplifier.

load line shown in Fig. 52. The waveforms show the current, voltage, and instantaneous power of one of the output transistors (Q1 or Q2 in Fig. 51) for operation into both a resistive and an inductive load at the clipping level. The out-of-phase current that results from an inductive load causes high instantaneous power dissipation which could cause second-breakdown in the output transistors. This condition can be avoided by use of load-line limiting and comparison of the reactive load line to the safe-area curves of the transistor. Distortion of the output signal that results when both output transistors are off (crossover distortion) can be avoided by use of the diodes D shown in Fig. 51 to provide a slight forward bias on both output transistors (class AB operation).

Fig. 53 compares a transformer-coupled class AB amplifier to a conjugate complementary amplifier. The elimination of a transformer in the conjugate complementary amplifier (and also in the quasi-complementary amplifier shown in Fig. 51) permits a lighter-weight, less costly construction and eliminates the phase shifts and stability problems normally

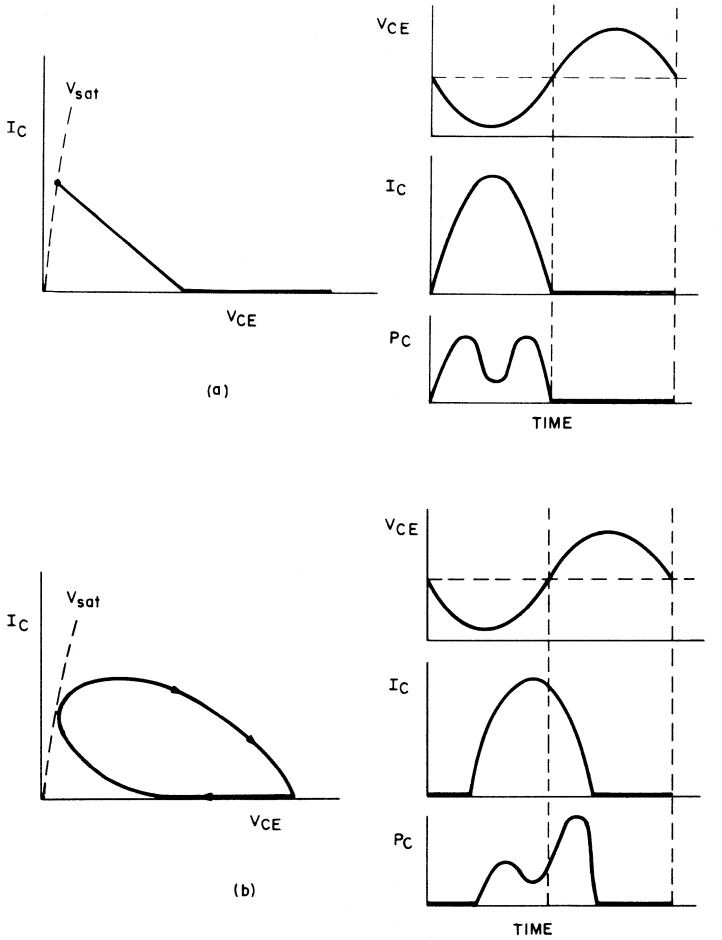


Fig. 52 — Typical load lines and operating waveforms for a class B amplifier: (a) resistive load; (b) inductive load.

associated with transformers. The main advantage of a transformer-coupled circuit is easier matching of transistor volt-ampere capability to various load impedances, servo motors, sonar transducers, and public-address sound-distribution systems.

Some important ways that transistor characteristics influence amplifier performance are as follows:

1. The frequency response of an amplifier is limited by the gain-bandwidth product f_T and the switching speed of the transistors.

2. Power output is limited by the safe area of the output transistors. The quality of amplification is largely a function of total harmonic distortion. Negative feedback is employed to reduce the harmonic distortion. Therefore, it would appear that high-gain devices would be preferred over lower-gain devices. However, higher-gain transistors normally have reduced second-breakdown capability because of accompanying narrower base widths. Narrower-base devices usually have a higher f_T as well. In general, a circuit designer should use a device with the lowest acceptable f_T for highest reliability.

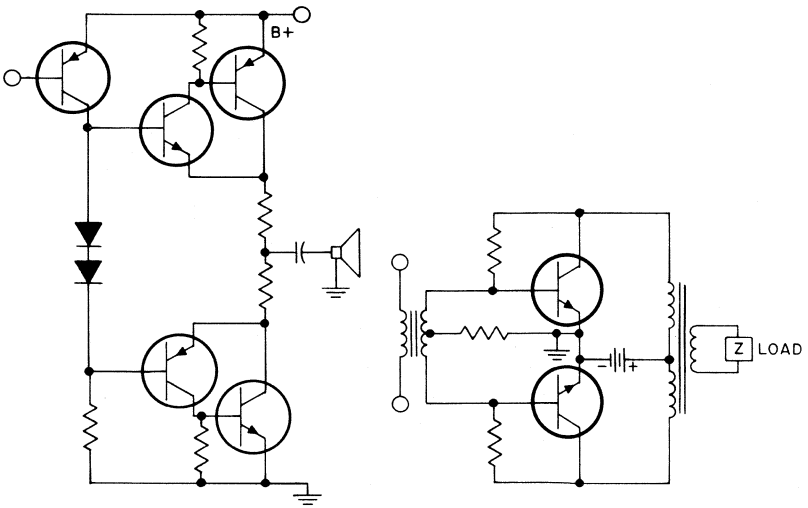


Fig. 53 – (a) Conjugate-complementary and (b) transformer-coupled class AB amplifiers.

SWITCHING REGULATOR

A switching regulator is used to maintain the output voltage V_O constant during variations in loading. Essentially, the regulator is an inductance-capacitance (LC) filter in series with a switch and a power source. By variation in the length of time the switch is on during each cycle, the amount of energy delivered to the filter can be controlled. The output voltage V_O is a function of this energy.

As shown in Fig. 54, Q1 is used in the switching mode; therefore, large power levels may be controlled with low loss. Because the output voltage of a switching regulator is not perfectly regulated, this circuit is often used as a preregulator.

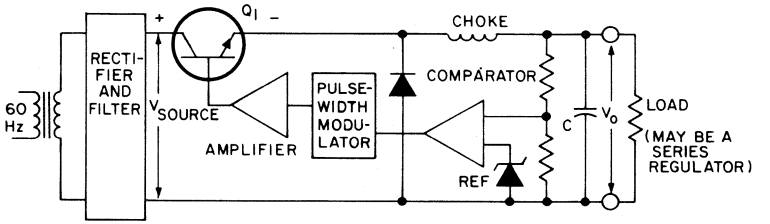


Fig. 54 – Switching regulator.

Typical operating waveforms for a switching regulator are shown in Fig. 55. The period T is constant; the transistor "on" time t, however, is variable. A differential amplifier compares the output voltage to a reference voltage, and that difference determines the "on" time t. The output voltage

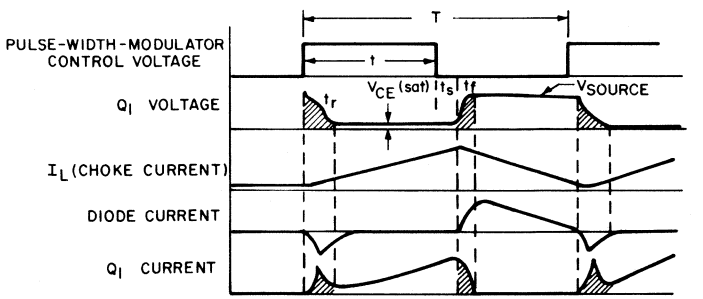


Fig. 55 – Typical operating waveforms for a switching regulator.

V_O is proportional to t for a given load. When Q1 is on, current increases linearly in the L part of the LC filter. When Q1 is off, the energy in L is transferred to C and the load. The commutating diode limits the voltage across Q1 to the supply voltage. When Q1 again turns on, the capacitance of the diode must be discharged. This discharge causes an initial spike in the collector current of Q1.

Some important characteristics of the switching-regulator performance are as follows:

1. The maximum operating frequency may be limited by the switching time of the transistor Q1.

2. The collector-to-emitter saturation voltage $V_{CE}(sat)$ and switching-time losses cause device dissipation and power loss. The power dissipation P_t in Q1 is determined as follows:

$$P_t = \frac{V_{CE}(sat)\, I_C(t)}{T} + \frac{E_{SW}\ (\text{rise and fall})}{T}$$

where t is the transistor "on" time, T is the period, I_C is the collector current in amperes, and E_{SW} is the energy absorbed by the output transistor during switching. The collector-to-emitter saturation voltage $V_{CE}(sat)$ and the transistor rise and fall times should be small to ensure low device dissipation.

3. The maximum output voltage is limited by the amount of voltage that Q1 can withstand without breaking down. Because the full source voltage appears across Q1 when it is off and the diode is on, the collector-to-emitter breakdown voltage V_{CEX} should be greater than the source voltage.

INVERTERS AND CONVERTERS

The main purpose of a power inverter or a power converter is to provide efficient conversion of power from a dc source, which may be a battery or a rectified line, to ac power (inverter) or dc power (converter) at some other voltage or current level. Fig. 56 shows a typical inverter/converter circuit. The converter or inverter may operate at any frequency consistent with the minimum transistor switching time and operating frequency of the transformer core. An additional function of an inverter may be to provide isolation.

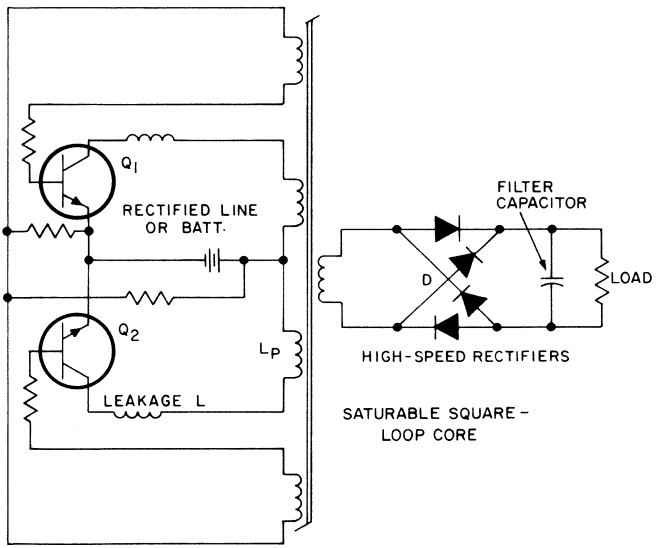


Fig. 56 – Typical inverter/converter.

Typical operating waveforms are shown in Fig. 57. Under steady-state conditions, at the start of a cycle current begins to rise linearly in the collector of the conducting transistor. Positive base drive is fed back, and the current increase continues until the transformer core saturates (a result of too many ampere-turns). At this point, the transformer primary inductance decreases suddenly, and collector current rises

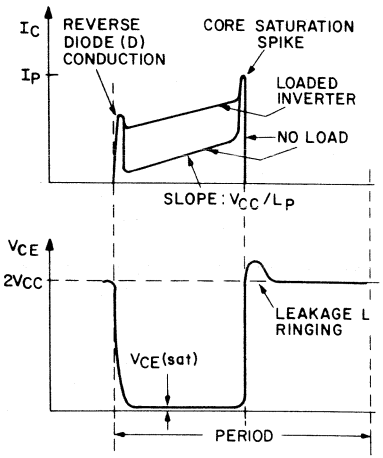


Fig. 57 – Typical waveforms for inverter/converter.

sharply. Base current, however, does not rise, and, therefore, the transistor is not maintained in saturation. The current then begins to decrease so that the direction of the rate of current with respect to time (di/dt) is changed. The change of direction of di/dt induces a negative voltage in the transformer feedback winding, and a positive voltage in the base winding of the other (OFF) transistor. As a result, the first transistor turns off, and the second transistor turns on. This action is repetitive and Q1 and Q2 are caused to conduct alternately. The discharge of the rectifier capacitance results in a small spike of collector current at the beginning of transistor conduction. Also, leakage inductance causes a voltage greater than twice the collector supply voltage V_{CC} to be developed across each transistor.

Fig. 58 shows several other types of inverters.

Some of the important characteristics of an inverter or converter are as follows:

1. The operating frequency is limited by the speed at which the transistor can switch, and by the transformer core used.

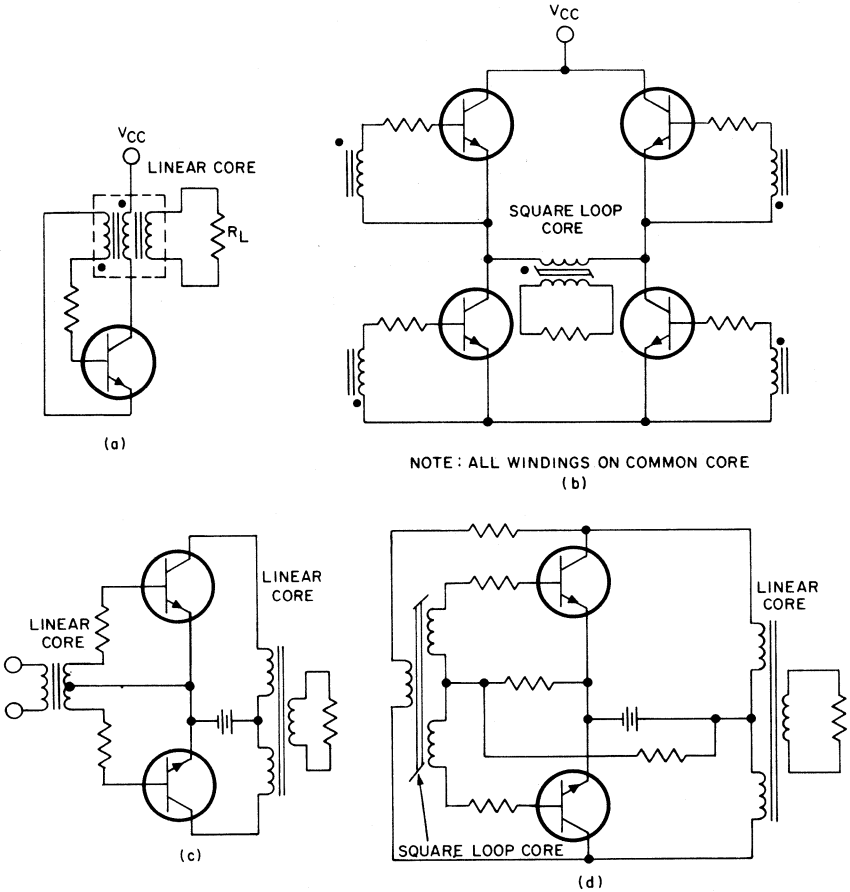


Fig. 58 – (a) Ringing choke inverter; (b) bridge inverter; (c) pulse-width-modulated inverter; and (d) two-transformer inverter.

2. Reactive loads may result in destructive loadlines. The survival of transistors in this situation depends upon the second-breakdown collector current $I_{S/b}$ and the second-breakdown energy $E_{S/b}$ of the individual transistors involved.

3. The power output and efficiency are enhanced if both the switching dissipation and the collector-to-

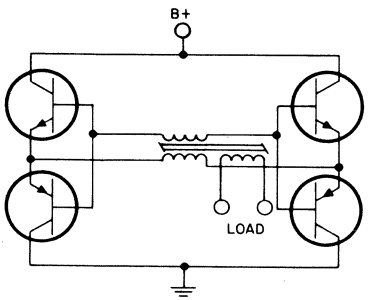
emitter saturation voltage $V_{CE(sat)}$ are maintained at low values. This relationship is apparent from the following equation for device dissipation:

$$P_t = \frac{I_p V_{CE(sat)}}{2} + \frac{E_{SW}}{T}$$

where P_t is the dissipation in one transistor, I_p is the current in the transformer primary, $V_{CE(sat)}$ is the collector-to-emitter saturation voltage, E_{SW} is the energy measured by graphical integration of the area under the power-versus-time curve during switching, and T is the period.

CIRCUIT APPLICATIONS OF COMPLEMENTARY TRANSISTOR PAIRS

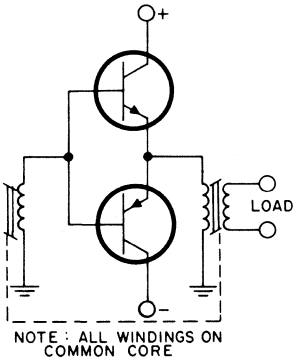
In recent years, increasing use has been made of n-p-n/p-n-p transistor pairs connected in complementary symmetry for both linear and switching circuit applications. Figs. 59, 60, and 61 show circuit diagrams and indicate advantages of the use of complementary transistor pairs in typical switching applications. Figs. 62 through 66 show the circuit connections and advantages for use of complementary transistor pairs in a number of popular linear applications.



ADVANTAGES:

1. Provides natural phase inversion.
2. Outstanding dc stability results from the fact that the bases of each complementary pair are directly connected.
3. Circuitry is simplified by elimination of three base windings on the transformer [compare with Fig. 58(b)].
4. Extended frequency capability as a result of reduced common-mode conduction.

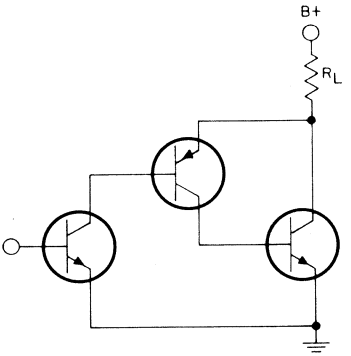
Fig. 59 – Use of complementary transistor pairs in a bridge inverter.



ADVANTAGES:

1. Reduced common-mode conduction.
2. Design of transformer is simplified.
3. No noncommutated leakage inductance.

Fig. 60 – Use of a complementary transistor pair in a push-pull inverter.

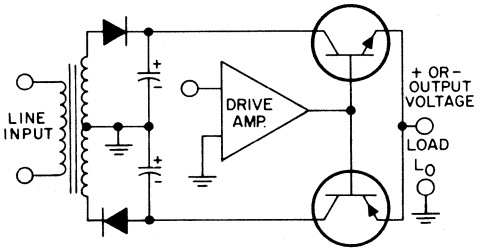


ADVANTAGES:

Ultra-high-gain n-p-n equivalent with only one V_{BE} offset.

Fig. 61 – High-gain n-p-n equivalent.

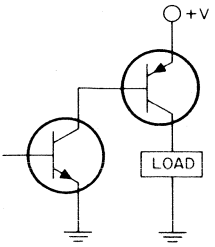
Table VIII lists several transistor pairs suitable for use as complementary driver or output devices in linear amplifiers. Table IX lists complementary pairs that can be used to provide the pass-transistor function in series regulators. Table X lists complementary pairs suitable for use in inverters and switching regulators.



ADVANTAGES:

1. Regulates positive and negative output voltages.
2. Low output impedance for each polarity of output voltage.

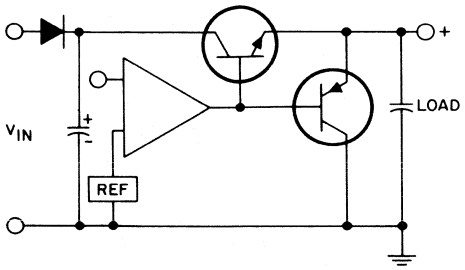
Fig. 62 – Complementary positive/negative series regulator.



ADVANTAGES:

Permits use of grounded load from positive supply in common-emitter mode.

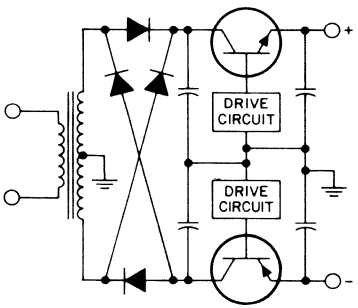
Fig. 63 – Complementary grounded load.



ADVANTAGES:

1. Capacitor discharges rapidly through the p-n-p transistor and, therefore, eliminates the need for an n-p-n/p-n-p transistor pair in the driver stage.
2. Uses common control.

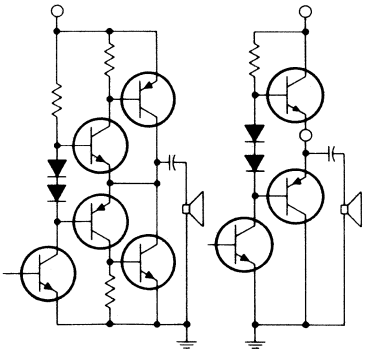
Fig. 64 – Use of a complementary transistor pair in a rapid-response series regulator.



ADVANTAGES:

1. May be used in place of two separate supplies.
2. Requires only one center-tapped transformer.
3. Uses only one full-wave bridge rectifier.

Fig. 65 – Complementary regulated supply.



ADVANTAGES:

1. Reduced circuit complexity.
2. Does not require separate phase inversion.
3. Outstanding dc stability
4. Extended frequency capability as a result of reduced common-mode conduction.

Fig. 66 – Complementary circuits for servo amplifiers, audio amplifiers, and wideband amplifiers.

Table VIII - Audio Linear Amplifiers (8-Ohm Load)

Power Output W	Type	Output Transistors		Driver Transistors		Predriver
		n-p-n	p-n-p	n-p-n	p-n-p	n-p-n
70	Quasi-Complementary	40636 (2N3055		40594 (2N5321)	40595 (2N5323)	40408 (2N2102)
40	Quasi-Complementary	40633 (2N5037)		40635 (2N2102)	40634 (2N4036)	
25	Quasi-Complementary	40632 (2N5497)		40635	40634	
12	Quasi-Complementary	40631 (2N5298)				
20	True Complementary	40627 (2N5497)	40626 (2N301) Ge	40628 (2N2102)		
12	True Complementary	40622 (2N5298)	40050 (2N301) Ge	40389 (2N2102)		
7	All Silicon, True Complementary	40620	40619	40616 (2N2102)		
60	Push-Pull Line Operation	2N3583		2N3583		
200	Push-Pull Modulator	2N5240				

Applications: Audio Power Amplifiers, Linear Modulators, Servo Amplifiers, Operational Amplifiers.

Table IX — Series Regulator Service — Pass Transistor

Conditions: with Preregulator, $I_C = I_O$, V_{CE} = Constant $\doteq 4\ V_{CE}$ (sat), $P_{MAX.} \doteq 4 I_O\ V_{CE}$ (sat)

Peak Output Voltage - V	Regulator Output Current - A				
	Up to 0.2	0.2 - 1	1 - 4	4 - 20	>20
10 - 60	[2N2102] [2N4036] 2N1482	[2N5321] [2N5323] [TA7289] [TA7270]	[2N3054] [2N5954] [2N5497] [TA7520]	2N5037 [2N3055] [TA7279] [2N3771]	2N3772 2N5575
60 - 150	40349	2N3441	2N4347 2N3442	2N4348 2N3773	2N5578
150 - 450	[2N3440] [2N5416]	[2N3585] [TA7410]	2N5840	2N5805 TA7007	TA7402

Notes for Table IX:

Brackets signify complementary pairs suitable for symmetrical ± power supplies

Preregulator limits voltage across pass unit; major constraints are maximum load current and $V_{CEO} > V$ pass for transient recovery time of preregulator.

Without preregulator, V_{CE} MAX. = V peak supply; major constraints are maximum load current and power dissipation under shorted output condition.

Table X - Inverter/Switching-Regulator Service

Frequency Range - kHz	Peak Voltage Required - V	Peak Primary Current Requirement - A				
		Up to 0.2	0.2 - 1	1 - 4	4 - 20	>20
	10 - 60	[2N4037* 2N2102]	[2N5323* 2N5321 2N5784*]	[2N5497# 2N5954* 2N3054]	2N5037# 2N3055 2N3772	
0.06 TO 12	60 - 150	2N1482	2N1486 2N2598# 2N3441	2N3442	[TA7279* 2N3773]	2N5580
	150 - 450	[2N5416* TA7134# 2N3440]	[TA7410* 2N3585]	2N5840	TA7007 2N5805	
12 TO 50	10 - 60	[2N4037* 2N2102]	[2N5323* 2N5321]			
	60 - 150			2N3879	2N3265 2N5039	TA7323 2N6032
	150 - 450	[2N5416* TA7134# 2N3440]	[TA7410* 2N3585]	2N5840	TA7007 2N5805	

* p-n-p

plastic

$V_{peak} = V_{CEX}$ rating

Push-pull inverters: $V_{peak} = 2.2\ V_{CC}$

Bridge inverters : $V_{peak} = 1.1\ V_{CC}$

Switching regulators: $V_{peak} = 1.1\ V_{source}$

Selection Charts

This section contains short-form descriptions of selected high-speed, high-voltage, high-power products. These recently announced types represent state-of-the-art refinements in structures and geometries that produce advances in speed, voltage, current, or power-handling capability. This section is intended only to highlight those products intended for use in advanced applications. More detailed data for the transistors listed, as well as for other RCA semiconductor devices, are provided in the individual RCA Technical Bulletins and the RCA semiconductor DATABOOK, SPD-100, or may be obtained from RCA Commercial Engineering, Harrison, N.J.

HIGH-SPEED TYPES

2N3879 (2N5202)

Package	TO-66
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	75 V
Collector Current (I_C) at $\beta = 10$	5 A
Power Dissipation (P_t)	35 W

Features

High speed; small size

Characteristics

Gain-Bandwidth Product (f_T) at $I_C = 0.5$ A . . . . . 60 MHz (min.)
Rise Time (t_r) or Fall Time (t_f) at $I_C = 4$ A . . . . . 400 ns (max.)

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	160	50	35	100
Switching Regulators	215	50	75	100
Linear Amplifiers	75	1000	35	100

Linear Series Regulators – to 5 A, 75 V

2N5038

Package TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$] ..... 90 V
Collector Current (I_C) at $\beta = 10$ ..... 15 A
Power Dissipation (P_t) ..... 140 W

Features

Multiple emitter sites; high speed

Characteristics

Gain-Bandwidth Product (f_T) at $V_{CE} = 10$ V, $I_C = 2$A ..... 60 MHz
Storage Time (t_{stg}) at $I_C = 10$ A, $V_{CE} = 30$ V ..... 0.7 μs
Rise Time (t_r) or Fall Time (t_f) at $I_C = 10$ A, $V_{CE} = 30$ V... 0.35 μs

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	575	50	45	100
Switching Regulators	1150	50	90	100
Linear Amplifiers	300	1000	45	100

2N5672

Package TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$] ..... 120 V
Collector Current (I_C) at $\beta = 10$ ..... 30 A
Power Dissipation (P_t) ..... 140 W

Features

High speed; high current; high voltage

Characteristics

Saturation Voltage [V_{CE} (sat)] at $I_C = 15$ A, $\beta = 12.5$ ..... 0.75 V
Gain-Bandwidth Product (f_T) at $I_C = 2$ A, $V_{CE} = 10$ V .... 50 MHz
Rise Time (t_r) or Fall Time (t_f) at $I_C = 15$ A, $V_{CE} = 30$ V... 0.5 μs
DC Current Transfer Ratio (h_{FE}) at $I_C = 20$ A ..... 20 min.

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	1500	50	60	100
Switching Regulators	1500	50	120	100
Linear Amplifiers	300	1000	60	100
Power Gates and Control Amplifiers – to 30 A, 120 V				

2N6033

Package	TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	120 V
Collector Current (I_C) at $\beta = 10$	50 A
Power Dissipation (P_t)	140 W

Features

Heavy leads (60 mils) for switching 50 A; high speed

Characteristics

Saturation Voltage [V_{CE} (sat)] at $I_C = 50$ A	1.5 V
Rise Time (t_r) at $I_C = 40$ A	1 μs
Storage Time (t_{stg}) or Fall Time (t_f) at $I_C = 40$ A	3 μs
Second-Breakdown Energy ($E_{S/b}$) at $I_C = 20$ A	62 mJ

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	2000	50	60	100
Switching Regulators	1500	50	120	100
Linear Amplifiers	300	1000	60	100

TA7279

Package	TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	100 V
Collector Current (I_C) at $\beta = 10$	15 A
Power Dissipation (P_t)	125 W

Features

High current (20 A rating); high speed ($f_T = 4$ MHz); p-n-p

Characteristics

Saturation Voltage [V_{CE} (sat)] at $I_C = 6$ A, $\beta = 10$	1 V (max.)
DC Current Transfer Ratio (h_{FE}) at $I_C = 10$ A, $V_{CE} = 4$ V	15 min.
On Time (t_{on}) at $I_C = 6$ A, $\beta = 10$	0.3 μs
Fall Time (t_f) at $I_C = 6$ A, $\beta = 10$	0.2 μs
Storage Time (t_{stg}) at $I_C = 6$ A, $\beta = 10$	0.33 μs

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	850	50	50	100
Switching Regulators	1400	50	100	100

TA7279 (Cont'd)

	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Linear Amplifiers	240	50	50	100
Linear Series Regulators – to 15 A, 100 V				

Comparison of TA7279 to High-Speed Types

	2N5038	TA7279	2N5672	
I_C at h_{FE} = 10	15	15	30	A
LV_{CEO}(sus)	90	100	120	V
f_T	60	4	50	MHz
$I_{S/b}$ Breakpoint Voltage	28	21	24	V
h_{FE}	20 (12A)	30 (6A)	20 (20A)	
Pellet Size.....	146x183	152x152	230x237	mils

Comparison of TA7279 to Single-Diffused Types

	2N3442	2N3055	TA3055	TA7279	2N3773	2N3772	
I_C at h_{FE} = 10	5	10	10	15	15	18	A
LV_{CEO}(sus)	140	60	100	100	140	60	V
$I_{S/b}$ Breakpoint Voltage	78	60	60	21	80	60	V
f_T	0.8	1	0.9	4	0.7	0.9	MHz
V_{CE} (sat) at I_{CE} = 10 A, h_{FE} = 10	1*	1.2	1	1.6	0.6	0.4	V
h_{FE}	20-70 (3A)	20-70 (4A)	20-70 (5A)	30-120 (6A)	15-60 (8A)	15-60 (10A)	

* at 5 amperes

HIGH-VOLTAGE TYPES

2N5240

Package TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$] ..... 300 V
Collector Current (I_C) at $\beta = 10$ ..... 3 A
Power Dissipation (P_t) ..... 100 W

Features

High voltage; excellent safe area

Characteristics

Safe Area at $V_{CE} = 150$ V ..... 0.67 A (100 W)
Gain-Bandwidth Product (f_T) at $V_{CE} = 10$ V, $I_C = 0.2$ A .... 5 MHz

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	300	25	150	100
Sonar & Ultrasonic Amplifiers	200	50	150	100
Linear Series Regulators – to 3 A, 300 V				
Vertical Deflection	20	0.06	82	100

2N5840

Package TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$] ..... 350 V
Collector Current (I_C) at $\beta = 10$ ..... 2 A
Power Dissipation (P_t) ..... 100 W

Features

High voltage for switching applications

Characteristics

Saturation Voltage [V_{CE} (sat)] at $I_C = 2$ A ..... 1.5 V
Rise Time (t_r) at $I_C = 2$ A ..... 0.6 μs
Fall Time (t_f) at $I_C = 2$ A ..... 1.75 μs
Switching Time (t_s) at $I_C = 2$ A ..... 0.35 μs

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	380	25	150	100
Switching Regulators	760	25	300	100

Circuit Applications (Cont'd)

Ignition – switches 5 A to 300 V
Phased-Array Radar - switches 5 A at $\beta = 8$ from 250 V

For Linear Service: **2N5240**	For Switching Service: **2N5840**
Features	
Outstanding breakdown capability (100 W at $V_{CE} = 150$ V)	Low saturation voltage (1.5 V at $I_C = 3$ A) Reverse-bias second breakdown measured on all devices
Similar Characteristics	
V_{CEO} (max.) at $I_C = 0.2$ A . . . . . 350 V	V_{CEO} (max.) at $I_C = 0.2$ A . . . . . 350 V
V_{CE} (sat) at $I_C = 2$ A, $I_B = 0.2$ A . . . . . 2.5 V	V_{CE} (sat) at $I_C = 2$ A, $I_B = 0.2$ A . . . . . 1.5 V
Outstanding Differences	
V_{BE} (sat) at $I_C = 2$ A . . . 3 V	V_{BE} (sat) at $I_C = 2$A . . . . . 2 V
$I_{S/b}$ at $V_{CE} = 150$ V . . 0.67 A	PRT at $V_{CE} = 40$ V . . . . . 2.5 A
$E_{S/b}$ . . . . . 1.6 mJ	$E_{S/b}$ . . . . . 0.45 mJ
Applications Requiring High $I_{S/b}$	**Applications Requiring Low V_{CE} (sat)**
Series Power Regulators	Switching Power Regulators
Modulators	Converters/Inverters–Ultrasonics
Linear Servo Amplifiers	Vertical Deflection
Sonar Amplifiers	Switching Bridge Amplifiers
VLF Applications	Inductive Ignition

TA7673

Package	TO-66
Collector-to-Emitter Voltage [LV_{CEO}(sus)]	350 V
Collector Current (I_C) at $\beta = 100$	2A
Power Dissipation (P_t)	45 W

Features

High Voltage for switching applications

2N6079 (cont'd)

Characteristics

Collector-to-Emitter Current (I_{CEX}) at V_{CC} = 450 volts and T_A = 25°C	0.5 mA
Saturation Voltage (V_{CE}(sat) at I_C = 4 A and I_B = 0.8 A	3 V
Rise Time (T_r) at I_C = 1.2 A	0.75 μs
Fall Time (t_f) at I_C = 1.2 A	0.75 μs

Circuit Applications

	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	380	25	150	100
Switching Regulators	760	25	300	100

Ignition – Switches 5 A to 300 V

Phased-Array Radar – Switches 5 A at β = 8 from 250 V

TA7007

Package	TO-3
Collector-to-Emitter Voltage [LV_{CEO}(sus)]	300 V
Collector Current (I_C) at β = 10	15 A
Power Dissipation (P_t)	100 W

Features

High voltage for switching applications

Fast switching ($t_r = t_f$ = 1 μs at I_C = 10 A)

Characteristics

Saturation Voltage [V_{CE} (sat)] at I_C = 10 A, β = 10	1 V
Second-Breakdown Current ($I_{S/b}$) at V_{CE} = 150 V	0.25 A

Circuit Applications

	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	2000	20	150	100
Switching Regulators	1500	20	300	100
Linear Amplifiers	250	300	150	100

Linear Series Regulators – to 15 A, 300 V

TA7402

Package	TO-63
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	300 V
Collector Current (I_C) at $\beta = 10$	20 A
Power Dissipation (P_t)	300 W

Features

High voltage
Excellent safe area (200 W at $V_{CE} = 150$ V, $I_C = 1.33$ A)

Characteristics

DC Current Transfer Ratio (h_{FE}) at $I_C = 15$ A, $V_{CE} = 10$ V	20
Second-Breakdown Energy ($E_{S/b}$) at L = 2 mH	150 mJ
Gain-Bandwidth Product (f_T) at $I_C = 1$ A	1 MHz

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	2500	20	150	100
Linear Amplifiers	600	20	150	100
Linear Series Regulators – to 15 A, 300 V				

For Linear Service: **TA7402**	For Switching Service: **TA7007**
Features	
High power dissipation (300 W)	High speed ($t_r = \mu s$ at $I_C = 10$ A)
High $I_{S/b}$ capability (200 W at $V_{CE} = 150$ V)	Low $V_{CE}(sat)$ (1.5 V at $I_C = 10$ A)
TO-63 stud package	
Characteristics	
V_{CEO} at $I_C = 0.2$ A . . . 300 V	V_{CEO} at $I_C = 0.2$ A. . . . . 300 V
h_{FE} at $I_C = 15$ A, $V_{CE} = 10$ V 20	V_{CE} (sat) at $I_C = 10$ A, $I_b = 0.1$ A . . . . . 1.5 V
	t_{on} at $I_C = 10$ A . . . 1.5 μs
	t_f at $I_C = 10$ A . . . . . 0.7 μs
$I_{S/b}$ at $V_{CE} = 150$ V . . 1.33A	$I_{S/b}$ at $V_{CE} = 150$ V . . . 0.22 A
f_T at $I_C = 1$ A, $V_{CE} = 4$ V . . . . . 1 MHz	f_T at $I_C = 1$ A, $V_{CE} = 5$ V . . . . . 5 MHz
Applications Requiring High $I_{S/b}$	**Applications Requiring Low V_{CE} (sat)**
Military Sonar Push-Pull Amplifiers	High-Power Off-Line Converters/ Inverters up to 2 kW Output
Linear High-Power Modulators up to 1.5 kW Output	Mercury Arc Ballasts (400 W)
Series Regulators	PCM Switching Modulators

2N5805

Package	TO-3
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	300 V
Collector Current (I_C) at $\beta = 10$	8 A
Power Dissipation (P_t)	110 W

Features

High voltage

Characteristics

Saturation Voltage [V_{CE} (sat)] at $I_C = 5$ A, $\beta = 10$	2 V
Gain-Bandwidth Product (f_T) at $I_C = 1$ A, $V_{CE} = 10$ V	15 MHz
On Time (t_{on}) at $I_C = 5$ A, $\beta_F = 10$	0.5 μs
Storage Time (t_{stg}) at $I_C = 5$ A, $\beta_F = 10$	3.5 μs
Fall Time (t_f) at $I_C = 5$ A, $\beta_F = 10$	2 μs

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	760	15	150	100
Switching Regulators	1400	15	300	100
Sonar Amplifiers	250	100	150	100

Linear Series Regulators – to 5 A, 300 V

HIGH-VOLTAGE n-p-n/p-n-p COMPLEMENTS

	2N3440 (n-p-n)	2N5415 (p-n-p)	
Package	TO-5	TO-5	
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	300	300	V
Collector Current (I_C) at $\beta = 10$	0.2	0.2	A
Power Dissipation (P_t)	10	10	W
Features			
Saturation Voltage [V_{CE} (sat)] at $I_C = 50$ mA	0.5 (at $\beta = 12$)	2.5 (at $\beta = 10$)	V
Second-Breakdown Current ($I_{S/b}$) at $V_{CE} = 200$ V	50	20	mA
Gain-Bandwidth Product (f_T)	25	35	MHz

Circuit Applications	Output Power W	Operating Frequency kHz	Case Temperature °C
Complementary Push-Pull Amplifiers	20	100	100
Complementary Inverters	12	50	100

+ Symmetrical Series Regulators – to 0.1 A, 300 V

	2N3585 (n-p-n)	TA7410 (p-n-p)	
Package	TO-66	TO-66	
Collector-to-Emitter Voltage [$LV_{CEO}(sus)$]	300	300	V
Collector Current (I_C) at β = 10.	1.2	1	A
Power Dissipation (P_t)	35	35	W
Features			
Second-Breakdown Current ($I_{S/b}$)	0.35 (at V_{CE} = 100 V)	1.75 (at V_{CE} = 20 V)	A
Gain-Bandwidth Product (f_T)	15	20	MHz
Saturation Voltage [V_{CE} (sat)]	1 (at I_C = 1 A)	2.5	V

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Complementary Push-Pull Amplifiers	60	100	300	100
Complementary Inverters	125	50	±150	100
± Symmetrical Series Regulators – to 1 A, 300 V			±300	100

VERY-HIGH-CURRENT TYPE

2N5578

Package	Mod. TO-3
Collector-to-Emitter Voltage [$LV_{VEO}(sus)$]	70 V
Collector Current (I_C) at β = 10	60 A
Power Dissipation (P_t)	300 W

Features

Hometaxial base
Special TO-3 case with heavy leads to handle 100 A
Multiple emitter sites to improve second breakdown and thermal performance
100-ampere selection capability
Availability with 1-inch stud adapter

Characteristics

Saturation Voltage [V_{CE} (sat)] at I_C = 40 A, β = 10 .... 1.5 V (max.)
Junction-to-Case Thermal Resistance ($\theta_{J\text{-}C}$) ..... 0.5 °C/W (max.)
Second-Breakdown Energy ($E_{S/b}$) at R_{BE} = 10Ω,

2N5578 (cont'd)

Circuit Applications	Output Power W	Operating Frequency kHz	Supply Voltage V	Case Temperature °C
Inverters	1750	10	35	100
Switching Regulators	3400	10	70	100
Linear Amplifiers	600	15	35	100
Linear Series Regulators – to 60 A, 70 V				

COMPLEMENTARY PAIRS

n-p-n Type	p-n-p Type	V_{CEO} V	I_C-A (at β = 10)	P_t W	Package
2N3440	2N5415	200	0.2	10	TO-5
2N3439	2N5416	300	0.2	10	TO-5
TA7739	2N5415	200	0.2	10	TO-5P▲, TO-5
TA7740	2N5416	300	0.2	10	TO-5P▲, TO-5
2N3585	TA7410	300	2.0	35	TO-66
2N3584	TA7719	250	2.0	35	TO-66
2N2102	2N4036	65	1.0	5	TO-5
2N3053	2N4037	40	1.0	5	TO-5
2N5320	2N5322	75	1.0	10	TO-5
2N5321	2N5323	50	1.0	10	TO-5
TA7554	TA7556	75	1.0	25	TO-5P▲
TA7555	TA7557	50	1.0	25	TO-5P▲
2N5294**	TA7520	75	1.5	30	VERSAWATT*
2N5296**	TA7639	65	2.0	30	VERSAWATT*
2N5298	TA7640	55	2.5	30	VERSAWATT*
2N5490**	2N6107	75	3.0	36	VERSAWATT*
2N5492**	2N6109	65	3.5	36	VERSAWATT*
2N5494**	2N6111	55	4.0	36	VERSAWATT*
2N5784	2N5781	80	2.5	10	TO-5
2N5785	2N5782	65	2.5	10	TO-5
2N5786	2N5783	45	2.5	10	TO-5
2N3441	2N5954	75	2.0	25	TO-66
2N3054	2N5955	55	3.0	25	TO-66
40250	2N5956	40	3.5	25	TO-66
2N4347	2N5954	75	4.0	40	TO-3, TO-66
2N3055	2N5955	60	6.0	40	TO-3, TO-66
40251	2N5956	40	6.0	40	TO-3, TO-66
2N3055**	TA7280	80	12.0	115	TO-3
2N4347	TA7279	100	4.0	100	TO-3
2N3772**	TA7280	80	17.0	125	TO-3
2N4348	TA7279	100	14.0	120	TO-3

* Plastic package (TO-66 equivalent). ▲ Plastic package (TO-5 equivalent).

RELIABILITY DATA

High-Speed Types

Test	Conditions	No. of Devices	Thousands of Hours or Cycles	No. of Failures
2N5038				
Operating Life	P_t = 6W, T_C = 125°C, Free Air	10	10	1
Operating Life	P_t = 6 W, T_C = 125°C, Free Air	25	16	0
Shelf Life	T_C = 200°C	24	24	0
Thermal Fatigue	P_t = 57 W, ΔT_C = 73°C	10	37	2
Constant Acceleration	5000 g	26	-	0
2N5672				
Operating Life	P_t = 60 W, T_C = 125°C	36	36	2
Shelf Life	T_C = 200°C	50	50	1
2N6032				
Operating Life	P_t = 60 W, T_C = 145°C	9	9	0
Shelf Life	T_C = 200°C	9	9	2
Temperature Cycle	-65°C to +200°C	10		2
Thermal Shock	0 to 150°C	10		0
Vibration Fatigue	20 g	7		0

High-Voltage Types

Test	Conditions	No. of Devices	Thousands of Hours or Cycles	No. of Failures
2N5840				
Operating Life	V_{CE} = 24 V, P_t = 50 W, T_c = 125°C	25	25	0

High-Voltage Types (Cont'd)

Test	Conditions	No. of Devices	Thousands of Hours or Cycles	No. of Failures
Shelf Life	T_c = 200°C	25	25	0
Centrifuge	5000 g, 1 min., X_1, X_2, Y_2	25		0
Temperature Cycle	Mil. Std. 1050.1	25		0
2N5240				
Operating Life	V_{CE} = 42 V, T_c = 125°C	28	28	0
Shelf Life	T_c = 200°C	52	52	0
Thermal Fatigue	P_t = 51 W, ΔT_c = 42°C	7	8.5	0
2N5805				
Operating Life	P_t = 50W, T_c = 125°C	30	51.5	1
Shelf Life	T_c = 200°C	20	5.6	1
Shock	1500 g	14		0
Vibration Fatigue	20g	14	1300	0
2N5415				
Operating Life	P_t = 1 W, Free Air	50	50	3
Shelf Life	T_c = 200°C	50	50	0

RCA MILITARY POWER TRANSISTORS

Type Numbers	MIL-S-19500
JANTX 2N1483, 2N1484, 2N1485, 2N1486	180
JANTX 2N3055	407
JANTX 2N3771, 2N3772	413
JAN 2N1479, 2N1480, 2N1481, 2N1482	207

RCA Military Power Transistors (Cont'd)

Type Numbers	MIL-S-19500
JAN 2N1483, 2N1484, 2N1485, 2N1486	180
JAN 2N1487, 2N1488, 2N1489, 2N1490	208
JAN 2N2015, 2N2016	248
JAN 2N3055	407
JAN 2N3439, 2N3440	368
JAN 2N3441	369
JAN 2N3442	370
JAN 2N3584, 2N3585	384
JAN 2N3771, 2N3772	413

All RCA power transistors which do not have JAN or JANTX versions are available for procurement as JAN or JANTX equivalent types tested in accordance with the following formats on a custom basis:

Inspection Lots Formed at Final Assembly Operation (Sealing)

A. Lots Proposed for JAN Types (non-TX)
   Inspection Tests to Verify LTPD (Group A, Group B, Group C)
   Review of Group A, B, and C Data for Accept or Reject Preparation for Delivery JAN

B. Lots Proposed for JANTX Types

100% Process Conditioning

1. High-temperature storage (24 hours min. at T_A = 200°C min.)
2. Thermal shock or temperature cycling (10 cycles at T_A = -65°C for 15 minutes, +25°C for 5 minutes, +200°C for 15 minutes, +25°C for 5 minutes)
3. Acceleration (Y_1 orientation, one time; 20,000g for TO-5, 10,000g or 5,000g for TO-3 or TO-66)
4. Hermeticity (fine-leak test, helium, 5 x 10^{-7} cm^3/second max.; gross-leak test, bubble, 100°C, 15 seconds)
5. Reverse bias (48 hours at T_A = +150°C, V_{CB} = 80% of V_{CBO} rating, I_E = 0)

100% Power Conditioning

1. Measurement of specified parameters (test and record h_{FE} and I_{CBO}, I_{CEX}, or I_{CEO})
2. Burn-in (168 hours at T_A = 25°C; P_T = 1 W for TO-5, 3 W for TO-66, 6 W for TO-3; no heat sink or forced air directly on the devices permitted; V_{CB} determined by BV_{CEO} as follows:

RCA Military Power Transistors (Cont'd)

Max. BV_{CEO} - V	V_{CB} - V
20	16
30	24
40	30
60	40
80	60
120	100
300	200

3. Measurement of specified parameters to determine delta and limit rejects.
4. Lot acceptance or rejection based on results of burn-in test (if more than 10% of devices subjected to burn-in fail in step 3, the entire lot is rejected for JANTX).

Inspection Tests to Verify LTPD (Group A, Group B, Group C)
Review of Group A, B, and C Data for Accept or Reject
Preparation for Delivery JANTX

RADIATION-HARD POWER TRANSISTORS

The recent emphasis on radiation effects on semiconductor devices has prompted considerable activity in the industry to develop radiation-hard devices for space and weapon environments. Although much of this work is classified, in general small-signal discrete devices, integrated circuits, and high-frequency devices are inherently more radiation-resistant than high-current, high-voltage discrete power devices. Because the performance of a system is limited by the weakest link, considerable attention has been given to increasing the hardness of power transistors.

The physical requirements necessary to produce the required electrical performance in power applications (such as high current, high voltage, and safe operating area) require design trade-offs because they are not naturally conducive to good radiation resistance. The effects of ionizing radiation (photocurrents) and of neutron damage [beta and $V_{CE}(sat)$ degradation] can be predicted, and compensating circuit-design considerations can be incorporated to neutralize or reduce these effects on the performance of the circuit. For

example, compensating techniques which produce current equal in magnitude but opposite in phase to photocurrents can be included, and beta degradation can be compensated by providing adequate base drive current.

RCA has developed power transistors which offer an optimized performance trade-off of radiation hardness, voltage, safe area, and power capability. For example, both photocurrent and voltage breakdown increase with increased collector resistivity because carrier lifetime is a function of resistivity. Collector resistivity, therefore, is fine-tuned to provide the maximum voltage breakdown possible with acceptable photocurrent performance. Post-radiation beta degradation is a function of base width, as is the frequency cutoff. Both of these characteristics are enhanced with decreasing base width. However, the safe-area capability is also a function of base width. Consequently, this parameter is fine-tuned to achieve optimum electrical performance and radiation hardness. Other techniques can be employed to enhance safe-area capability, such as the introduction of various amounts of ballasting.

With proper attention to optimizing the various trade-offs, power devices provide acceptable electrical performance along with radiation-hardness levels which allow control by "state-of-the-art" circuit techniques.

A number of the transistors referred to in this Manual are developmental types (identified by the TA prefix to the type number designation). Developmental-type devices and materials are intended for engineering evaluation. The type designations and data are subject to change, unless otherwise arranged. No obligations are assumed for notice of change or future manufacture of these devices or materials.

Other RCA Technical Manuals

	Price*†
RCA Transistor, Thyristor, & Diode Manual (SC-15)	$2.50
RCA Linear Integrated Circuits (IC-42)	$2.50
RCA COS/MOS Integrated Circuit Manual (CMS-270)	$2.50
RCA Solid-State Hobby Circuits Manual (HM-91)	$1.95
RCA Receiving-Tube Manual (RC-27)	$2.00
RCA Electro-Optics Handbook (EOH-10)	$2.50
RCA Photomultiplier Manual (PT-61)	$2.50
RCA Transmitting Tubes (TT-5)	$1.00
RCA Transistor Servicing Guide (TSG-1673)	$3.50
RCA Silicon Controlled Rectifier Experimenter's Manual (KM-71)	$0.95

* Prices shown apply in U.S.A. and are subject to change without notice.

† Suggested Price.

Copies of these publications may be obtained from your RCA distributor or from RCA Commercial Engineering, Harrison, N. J. 07029.

RCA | Solid State Division | Somerville, N. J. 08876